P516328.PDF [Page: 4 of 106]

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Military Voice Services over Wireless ATM Networks: Performance Analysis of FEC Schemes for ATM Transport Over Wireless Links

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P516328.PDF [Page: 5 of 106]

Abstract

Wireless ATM was designed to extend the support of broadband, multimedia services provided in fixed ATM networks to the wireless/mobile environment in a seamless and efficient manner. It is a candidate wireless networking technology for future tactical military networks which have adopted ATM in the core network. The bandwidth-limited, error-prone nature of wireless links poses significant challenges in the design of wireless ATM.

This report is part of a study on the feasibility of military digital voice services over wireless ATM networks and is concerned with the impact of wireless link errors on the performance of ATM. The work presents a review of various error-control schemes proposed for the efficient transport of ATM over point-to-point wireless links. Due to the strict latency requirements of voice applications, only error-control schemes based on Forward Error Correction are considered. The performance of these schemes is analyzed for the random-error channel and for the Gilbert-Elliott burst-error channel.

P516328.PDF [Page: 6 of 106]

Résumé

Le mode de transfert asynchrone (MTA) sans fil a été mis au point pour étendre les services multimédias à large bande assurés par des réseaux MTA fixes au milieu des communications mobiles et sans fil de manière efficace et transparente. C'est un choix approprié de mise en réseau sans fil qui pourrait être employée dans l'avenir pour les réseaux militaires tactiques dont le réseau fédérateur fonctionne déjà en MTA. La faible largeur de bande et la probabilité d'erreurs associées aux liaisons sans fil opposent toutefois de sérieux obstacles à la conception de réseaux MTA sans fil.

Le présent rapport fait partie d'une étude de la faisabilité de services vocales à usage militaire empruntant des réseaux MTA sans fil. Il porte sur l'incidence des erreurs survenant au niveau de la liaison sans fil sur la qualité de transmission assurée par le MTA. L'auteure y passe en revue diverses méthodes de détection d'erreurs proposées pour le transport efficace des cellules MTA par l'intermédiaire de liaisons sans fil point à point. Vu l'extrême brièveté des retards admissibles dans le contexte d'applications vocales, les seules méthodes de détection d'erreurs examinées sont celles qui se fondent sur la correction d'erreur sans voie de retour (aussi dite correction d'erreur directe ou CED). L'auteure analyse l'efficacité de ces méthodes à l'égard d'un canal où les erreurs sont aléatoires et d'un canal façonné sur le modèle Gilbert-Elliott, où les erreurs se produisent par paquets.

Executive Summary

The adoption of ATM-based wireless transport architectures in future broadband wireless networks facilitates the seamless extension of fixed ATM network capabilities to the wireless environment. For this reason, wireless ATM is an attractive candidate technology for tactical networks which have adopted ATM in the core network. At the same time, the transport of ATM cells over wireless links raises challenging performance issues due to incompatibilities of the ATM technology and the wireless medium transmission characteristics.

ATM technology was originally designed for transport over high-speed, fiber-optic links, with low bit-error rates—typically of the order of 10^{-10}—and has, therefore, limited error-control capabilities. Wireless links have limited bandwidth and are characterized by high error rates—with errors occurring both in a random and burst manner—and time-varying behavior. Wireless link errors can severely degrade the performance of ATM and the Quality of Service (QoS) provided to ATM applications.

This work investigates the effect of bit errors on the transport of ATM over point-to-point wireless links. Of particular interest are Line-of-Sight (LOS) microwave links which are prevalent in tactical communications. The study analyzes the performance of mechanisms proposed for error control over the random-error channel and over a burst-error channel modeled by the Gilbert-Elliott channel model. The error-control mechanisms are based on Forward Error Correction (FEC) and more specifically on block codes such as the Reed-Solomon (RS) and the Bose-Chaudhuri-Hocquenghem (BCH) codes.

Block codes are applied to standard ATM cells to form wireless ATM cells which are transmitted over the radio channel. The error-control schemes under consideration are distinguished into three categories: i) schemes where a block code is applied to the entire standard ATM cell, ii) schemes where the ATM cell header and payload are protected individually by different block codes, iii) schemes which make use of duplicate cell headers.

Key performance measures of interest for the evaluation of these schemes are the Cell Loss Ratio and the error rate of the information delivered to the ATM layer which capture the Quality of Service (QoS) provided to the ATM applications. The work herein is primarily concerned with the performance of voice applications which are quite tolerant to loss but sensitive to delays.

Most of the performance results were derived by using analytical methods based on probability theory. The complexity associated with obtaining simulation results for low bit-error rates is prohibitively high. However, some simulation results were obtained by using a modified version of CRC LINKSIM with a simplified channel model.

Numerical results indicate that an error-control scheme that uses a (56,32) BCH code for the header and a (429,384) BCH code for the payload can adequately meet the performance requirements of voice over the random-error channel. In the case of the burst-error channel, the best performance with respect to Cell Loss Ratio was exhibited by a duplicate-header scheme which uses compressed headers encoded by using a (51,24) BCH code.

DREO-TR-2001-058, CRC-RP-2001-03, *Performance Analysis of FEC Schemes for ATM Transport over Wireless Links*, Sophia Tsakiridou, CRC, VPNT-RNS, Ottawa

P516328.PDF [Page: 8 of 106]

Sommaire

L'utilisation d'architectures de transport sans fil reposant sur le mode de transfert asynchrone (MTA) dans les réseaux sans fil à large bande facilite l'extension homogène des capacités des réseaux MTA fixes au milieu des communications sans fil. Le MTA sans fil constitue pour cette raison une technique attrayante pour les réseaux tactiques dont le réseau fédérateur fonctionne déjà en MTA. L'incompatibilité du MTA et des caractéristiques de transmission du sans-fil pose toutefois de sérieux points d'interrogation quant à l'efficacité du transport de cellules MTA par l'intermédiaire de liaisons sans fil.

Le MTA a été mis au point pour le transport par liaisons optiques à grande vitesse et faible taux d'erreur sur les bits—typiquement de l'ordre de 10^{-10}—, et ses capacités de correction d'erreurs sont donc limitées. Or, les liaisons sans fil occupent une faible largeur de bande et se caractérisent par un taux d'erreur élevé et un comportement qui varie selon le moment. Les erreurs survenant au niveau de la liaison sans fil, qui peuvent se produire de façon aléatoire ou par paquets, peuvent entraîner une détérioration considérable de la transmission MTA et de la qualité de service assurée aux applications MTA.

L'auteure examine l'effet des erreurs sur le transport de cellules MTA par l'intermédiaire de liaisons sans fil point à point. Elle se penche en particulier sur les liaisons hertziennes en visibilité directe, qui sont les plus employées pour les communications tactiques. Elle analyse l'efficacité de méthodes proposées pour la détection d'erreurs dans un canal où les erreurs sont aléatoires et dans un canal façonné sur le modèle Gilbert-Elliott, où les erreurs viennent par paquets. Les méthodes examinées reposent sur la correction d'erreurs sans voie de retour (aussi dite correction d'erreur directe ou CED) et, plus précisément, sur des codes de blocs, tels les codes Reed-Solomon et Bose-Chaudhuri-Hocquenghem (BCH).

Les codes de blocs sont appliqués aux cellules MTA standard pour former des cellules MTA sans fil, qui sont transmises dans le canal radio. Les méthodes de détection d'erreurs analysées se répartissent en trois catégories : i) celles où l'on applique un code de blocs à la cellule MTA standard entière; ii) celles où l'en-tête de la cellule et les données utiles qu'elle renferme sont protégées par des codes de blocs distincts; iii) celles qui utilisent le dédoublement des en-têtes de cellules.

Les mesures de la qualité de transmission présentant le plus d'intérêt pour l'évaluation de ces méthodes sont le taux de suppression de cellules et le taux d'erreurs de l'information livrée à la couche MTA, qui exprime la qualité de service assurée aux applications MTA. L'auteure s'est arrêtée surtout à la qualité de transmission des applications vocales qui supportent assez bien les suppressions, mais sont très sensibles aux retards.

Les résultats dont il est fait état sont pour la plupart issus de l'application de méthodes analytiques fondées sur la théorie des probabilités. La simulation de faibles taux d'erreur sur les bits est en effet trop complexe pour être réalisable. L'auteure est néanmoins parvenue à obtenir certains résultats de simulation en utilisant une version modifiée du système LINKSIM du CRC et un modèle de canal simplifié.

D'après les chiffres obtenus, l'utilisation d'une méthode de détection d'erreurs employant un code BCH (56,32) pour l'en-tête et un autre code BCH (429,384) pour les données utiles serait adéquate pour assurer la qualité de transmission vocale requise dans le canal où les erreurs sont aléatoires. Dans le canal où les erreurs surviennent par paquets, la méthode ayant donné les meilleurs résultats du point de vue de la suppression de cellules était celle qui supposait le dédoublement de l'en-tête et le codage des en-têtes comprimes à l'aide d'un code BCH (51,24).

DREO-TR-2001-058, CRC-RP-2001-03, *Performance Analysis of FEC Schemes for ATM Transport over Wireless Links*, Sophia Tsakiridou, CRC, VPNT-RNS, Ottawa

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P516328.PDF [Page: 10 of 106]

Contents

1 Effect of Channel Errors on ATM Performance 1
1.1 Introduction . . . 1
1.2 Header Error Control . . . 2
1.2.1 Header Error Control (HEC) Mechanism . . . 2
1.2.2 Effect of Channel Errors on the HEC Mechanism . . . 3
1.3 Cell Delineation . . . 5
1.3.1 Cell Delineation Mechanism . . . 5
1.3.2 Effect of Channel Errors on the Cell Delineation Mechanism . . . 6

2 FEC-Based Error Control for Wireless ATM 9
2.1 Introduction . . . 9
2.2 NATO PG/6 Proposal . . . 10
2.2.1 System Description . . . 10
2.2.2 Performance Over the Random-Error Channel . . . 11
2.3 NTT Proposal . . . 14
2.3.1 System Description . . . 14
2.3.2 Performance Over the Random-Error Channel . . . 14
2.4 DERA Proposal . . . 18
2.4.1 System Description . . . 18
2.4.2 Performance Over the Random-Error Channel . . . 18

3 Approaches for Adapting ATM to the Wireless Medium 22
3.1 Yurie Approach . . . 22
3.1.1 LANET Frame Structure . . . 22
3.1.2 Cell Delineation Mechanism . . . 23
3.1.3 Multiple Redundancy Addressing . . . 24
3.1.4 Payload Encoding . . . 25
3.1.5 Comments . . . 25
3.2 GTE Tactical ATM . . . 26
3.2.1 Wireless Environment/System Characteristics . . . 26
3.2.2 Key Features . . . 26
3.2.3 Tactical ATM Frame Structure . . . 27
3.2.4 Error-Control Coding . . . 28

4 Recommendations for Error Control Over the Random-Error Channel 31

5 Performance Over the Markov Channel 32
5.1 Introduction . . . 32
5.1.1 Channel Model Description . . . 32
5.1.2 Performance Analysis . . . 33
5.1.3 Performance Measures . . . 36
5.1.4 Performance Over the Gilbert-Elliott Channel . . . 38
5.2 Standard ATM . . . 40
5.2.1 Error-Detection Mode . . . 40
5.2.2 Error-Correction Mode . . . 43
5.3 NATO PG/6 Proposal . . . 45

5.3.1 Performance of Cell RS Codes 45
5.3.2 Performance of Cell BCH Codes 48
5.3.3 Performance Comparison of RS and BCH Codes 53
5.4 Combination Header/Payload FEC 56
5.4.1 Performance of (50,32) BCH Header/(420,384) BCH Payload Codes . . . 57
5.4.2 Performance of (56,32) BCH Header/(429,384) BCH Payload Codes . . . 58
5.4.3 Performance of (82,40) BCH Header/(421,376) BCH Payload Codes . . . 59
5.4.4 Performance of (56,32) BCH Header/(224,192) BCH Payload Codes . . . 60
5.4.5 Performance Comparison of Combination Header/Payload FEC 62
5.5 Duplicate-Header Scheme 67
5.5.1 Performance of DERA Scheme in Error-Detection Mode 67
5.5.2 Performance of DERA Scheme in Error-Correction Mode 74
5.5.3 Performance of DERA Scheme with Compressed Headers 75
5.5.4 Performance of Duplicate-Header Scheme with BCH-Encoded Headers . . 77
5.5.5 Performance of Duplicate-Header Scheme with BCH-Encoded Compressed Headers 78
5.5.6 Performance Comparison of Duplicate-Header Schemes 80

6 Recommendations for Error Control Over the Markov Error Channel **83**

A Derivation of probabilities P_{dis} and P_{und} **87**

References **88**

List of Figures

1 *HEC operation state transition diagram.* . . . 2
2 *HEC verification flow diagram.* . . . 3
3 *HEC performance in mixed and detection modes.* . . . 4
4 *CLR performance in mixed and detection modes.* . . . 4
5 *Cell delineation state diagram.* . . . 5
6 *T_{sync} and T_{acq} for the ITU-T recommended cell delineation mechanism.* . . . 7
7 *Frame structure for Synchronous Transport Signal Level 1 (STS-1).* . . . 8
8 *Block structure of wireless ATM cell for the PG/6 proposal.* . . . 10
9 *PG/6 error-control scheme performance.* . . . 12
10 *BCH code performance.* . . . 13
11 *Block structure of wireless ATM cell for the NTT proposal.* . . . 14
12 *Header BCH code CLR performance.* . . . 15
13 *Payload BCH code Residual BER performance.* . . . 16
14 *DERA link hardening scheme.* . . . 18
15 *Wireless ATM cell structure proposed for voice transmissions.* . . . 18
16 *Duplicate-header scheme performance – Header-error detection case.* . . . 19
17 *Duplicate-header scheme performance – Header-error correction case.* . . . 20
18 *LANET frame structure.* . . . 22
19 *LANET cell delineation state diagram.* . . . 23
20 *LANET cell delineation algorithm performance.* . . . 24
21 *Tactical ATM frame structure.* . . . 27
22 *Channel model.* . . . 34
23 *Data block structure for performance analysis.* . . . 35
24 *State transition diagram of Gilbert-Elliott channel model.* . . . 38
25 *Sample realization of process $\{e_n\}_{n\geq 1}$.* . . . 38
26 *Analytical results for standard ATM over the GE channel in HEC detection mode.* 40
27 *Analytical results for standard ATM over the GE channel in HEC detection mode.* 42
28 *Analytical results for standard ATM over the GE channel in HEC correction mode.* 42
29 *Analytical results for standard ATM over the GE channel in HEC detection and correction modes.* . . . 43
30 *Analytical results for the PG/6 error-control scheme over the GE channel.* . . . 46
31 *Analytical and simulation results for the (59,53) RS code over the GE channel.* 47
32 *Analytical results for the (469,424) BCH and (478,424) BCH codes over the GE channel.* . . . 49
33 *Comparison of analytical results for the (469,424) BCH and (478,424) BCH codes over the GE channel.* . . . 50
34 *Analytical and simulation results for the (469,424) BCH code over the GE channel.* 51
35 *Analytical and simulation results for the (478,424) BCH code over the GE channel.* 51
36 *Analytical and simulation results for the (469,424) BCH and (478,424) BCH codes over the GE channel.* . . . 52
37 *Comparison of analytical results for the RS and BCH codes over the GE channel.* 53
38 *Comparison of simulation results for the RS and BCH codes over the GE channel.* 55
39 *Analytical results for the (50,32) BCH header/(420,384) BCH payload codes over the GE channel.* . . . 57

P516328.PDF [Page: 13 of 106]

40 *Analytical results for the (56,32) BCH header/(429,384) BCH payload codes over the GE channel.* . . . 58
41 *Analytical results for the (82,40) BCH header/(421,376) BCH payload codes over the GE channel.* . . . 59
42 *Analytical results for the combination (56,32) BCH header code and (224,192) BCH payload code over the GE channel.* . . . 61
43 *Performance comparison of CLR for combination header/payload BCH codes.* . . . 62
44 *Performance comparison of CER for combination header/payload BCH codes.* . . . 63
45 *Performance comparison of PER for combination header/payload BCH codes.* . . . 63
46 *Performance comparison of PBER for combination header/payload BCH codes.* 64
47 *Performance comparison of CLR for combination header/payload BCH codes.* . . . 65
48 *Performance comparison of CER for combination header/payload BCH codes.* . . . 65
49 *Performance comparison of PER for combination header/payload BCH codes.* . . . 66
50 *Performance comparison of PBER for combination header/payload BCH codes.* 66
51 *Wireless ATM cell structure for the DERA error-control proposal.* . . . 67
52 *Analytical results for the DERA duplicate-header scheme over the GE channel in HEC detection mode (payload size = 384).* . . . 68
53 *Analytical results for the DERA duplicate-header scheme over the GE channel in HEC detection mode for different values of payload size N_1.* . . . 71
54 *Wireless ATM cell structure for the duplicate-header control scheme (scenario 2).* 72
55 *Analytical results for different scenarios of the duplicate-header scheme over the GE channel in HEC detection mode (payload size = 384).* . . . 72
56 *Analytical results for the duplicate-header scheme (scenario 2) over the GE channel in HEC detection mode for different values of payload size N_1.* . . . 73
57 *Analytical results for the DERA duplicate-header scheme over the GE channel in HEC correction mode (payload size = 384).* . . . 74
58 *Analytical results for the DERA duplicate-header scheme over the GE channel in HEC detection mode (compressed headers).* . . . 75
59 *Analytical results for the DERA duplicate-header scheme over the GE channel in HEC correction mode (compressed headers).* . . . 76
60 *Analytical results for the duplicate-header scheme over the GE channel with (56,32) BCH header code.* . . . 77
61 *Analytical results for the duplicate-header scheme over the GE channel with (48,24) BCH header code.* . . . 78
62 *Analytical results for the duplicate-header scheme over the GE channel with (51,24) BCH header code.* . . . 79
63 *Performance comparison of CLR for duplicate-header schemes.* . . . 80
64 *Performance comparison of CER for duplicate-header schemes.* . . . 81
65 *Performance comparison of PER for duplicate-header schemes.* . . . 81
66 *Performance comparison of PBER for duplicate-header schemes.* . . . 82
67 *CLR performance comparison.* . . . 83
68 *CER performance comparison.* . . . 84
69 *PER performance comparison.* . . . 84
70 *PBER performance comparison.* . . . 85
71 *Performance comparison.* . . . 86

P516328.PDF [Page: 14 of 106]

List of Tables

1 *Block code performance.* 13
2 *Header BCH code performance.* 15
3 *Payload BCH code performance.* 16
4 *Separate header and payload encoding – BCH code performance.* 17
5 *BCH header and payload code performance.* 30
6 *Block code performance over the random-error channel.* 31
7 *Comparison of analytical results for the RS and BCH codes over the GE channel.* 54

1 Effect of Channel Errors on ATM Performance

1.1 Introduction

ATM was designed for high-speed, highly reliable fiber-optic links. Wireless links, however, are typically characterized by limited bandwidth, high error rates—with errors occurring both in a random and burst manner—and time-varying behavior. The impact of transmission link errors on the performance of ATM is addressed in this section with focus on high error rates which are typical of wireless links.

The adaptation of ATM to the physical transmission medium is performed by the physical layer interface. ATM physical layer standards exist for media such as optical fiber and coaxial cable, while protocols for lower rate, unreliable media are currently under development. In principle, existing physical layer protocols can be used for transmission over wireless links provided that adequate bandwidth is available. However, the protocol performance and consequently the performance of ATM may be significantly impaired by high error rates.

Key physical layer functions affected by errors are *Header Error Control* and *Cell Delineation*, as well as *Frame Synchronization*, whenever a frame-based transmission format is used. These functions are provided for by the Transmission Convergence (TC) sublayer of the physical layer interface. Header error control protects the ATM cell against errors in the header. It is also used in the cell delineation process. Cell delineation and frame synchronization are responsible for identifying cell and frame boundaries, respectively.

The ATM header error control and cell delineation mechanisms, which have been designed for low-error-rate transmission media, are susceptible to transmission errors. Bit errors in the ATM cell header may result in the loss of ATM cells, either directly due to the HEC mechanism, or indirectly due to the loss of cell synchronization by the cell delineation process which relies strongly on the integrity of the cell header. Cell synchronization fails when an adequate number of consecutive corrupted headers is detected. The loss of cell synchronization results in the discarding of consecutive ATM cells during the process of acquiring synchronization.

Transmission errors degrade the ability of the cell delineation process to maintain and acquire cell synchronization by inducing false loss of synchronization and by increasing the acquisition time required to regain synchronization following a loss-of-synchronization event.

When ATM cells are transported by using frame-based transmission formats such as the Synchronous Digital Hierarchy (SDH) or the Plesiochronous Digital Hierarchy (PDH), the performance of the frame synchronization mechanism may be affected by errors in the frame structure. Much as in the case of the cell delineation process, transmission errors affect the ability of the framing process to maintain and acquire frame synchronization. The loss of frame synchronization causes the loss of information bits for the duration of the frame acquisition time and may, therefore, result in the discarding of successive ATM cells, which, in turn, may affect the cell delineation process.

The impact of transmission errors on the HEC and cell delineation mechanisms is addressed in detail in the following subsections.

1.2 Header Error Control

Originally designed for fiber-optic transmission links characterized by extremely low bit-error rates of the order of 10^{-10}, ATM has limited error-control capabilities. Error control is applied to the cell header only, for protection against cell misrouting, while the control of errors in the cell payload is delegated to protocol layers higher than the ATM layer.

1.2.1 Header Error Control (HEC) Mechanism

A (40,32) shortened cyclic code with generator polynomial $g(x) = x^8 + x^2 + x + 1$ is used to protect the four bytes of information carried in the cell header[1]. Parity-check bits occupy the fifth byte in the cell header, the Header Error Control (HEC) field. The code has the capability to correct single-bit errors and to detect all double-bit errors and a large fraction of multiple-bit errors.

The ATM HEC decoder at the receiver uses a two-state correction/detection process with state transition diagram shown in Fig. 1. In correction mode, single-bit header errors are cor-

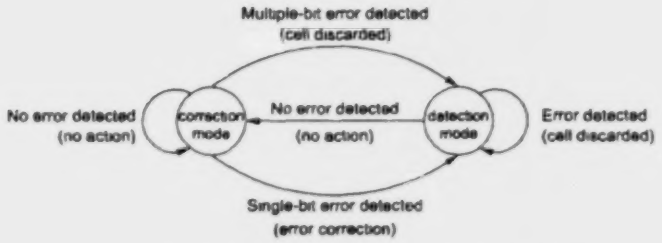

Figure 1: HEC operation state transition diagram.

rected while detected multiple-bit header errors result in cell discard. In both cases, a detected error forces a transition from correction to detection mode. In detection mode, no error correction takes place and all cells with detected header errors are discarded. A transition from detection back to correction mode does not take place unless a header with no errors is detected. That is, in mixed (correction/detection) mode operation of the HEC decoder, when a number of consecutive headers are found in error, all but the first one are discarded. This mode of operation takes into consideration the fact that there exists a small probability of errors occurring in long bursts in fiber-optic links. The ATM Forum UNI 3.1 document makes the implementation of the detection mode mandatory while the implementation of the correction mode is optional [1, p. 15].

The performance of the HEC mechanism in the presence of random-channel errors is discussed in the following subsection.

[1]The ATM cell header contains the Generic Flow Control (GFC), Virtual Path Identifier (VPI), Virtual Circuit Identifier (VCI), Payload Type Indicator (PTI), Cell Loss Priority (CLP) and Header Error Control (HEC) fields. The VPI/VCI fields carry the address information used for routing the ATM cells through the network.

1.2.2 Effect of Channel Errors on the HEC Mechanism

According to the HEC operation, there are three possible outcomes of a HEC check when a cell with header errors is received:

- the cell may be discarded,
- the cell may be forwarded to the ATM layer with no header errors following successful error correction, and,
- the cell may be forwarded to the ATM layer with undetected header errors, including errors due to incorrect correction in mixed mode.

These three possible outcomes are depicted in Fig. 2.

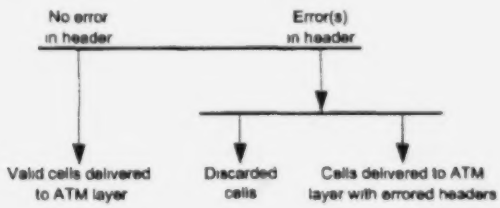
No error in header
Error(s) in header
Valid cells delivered to ATM layer
Discarded cells
Cells delivered to ATM layer with errored headers

Figure 2: HEC verification flow diagram.

Cells with undetected header errors in the VPI/VCI fields will be misrouted and eventually lost. In addition, these cells may affect the integrity of other connections. For example, the undetected change of the VPI/VCI fields to the address of another connection will result in cell misinsertion.

The performance of ATM HEC mechanism with respect to cell loss in the presence of link errors can be captured by

- the probability that a cell is discarded, P_{dis}, and,
- the probability that a cell header error is undetected, P_{und}.

Numerical results for P_{dis} and P_{und} versus the channel Bit-Error Rate (BER) p in mixed and pure detection modes are presented in Fig. 3. Channel errors are assumed to be randomly distributed. These results have been obtained by applying the methodology described in [2, p. 18]; the codeword weight distribution for the HEC CRC code is provided in [3]. Note that the probability of cell discard P_{dis} is lower in mixed than in detection mode, due to single-bit error correction in mixed mode. This, however, is achieved at the expense of a higher undetected error rate P_{und} in mixed mode, caused by incorrect error corrections, as shown in Fig. 3.

The Cell Loss Ratio (CLR) QoS parameter is easily obtained from

$$\text{CLR} = \Pr\{\text{cell is lost}\} = \frac{\text{Lost Cells}}{\text{Total Transmitted Cells}} = P_{dis} + P_{und}; \quad (1)$$

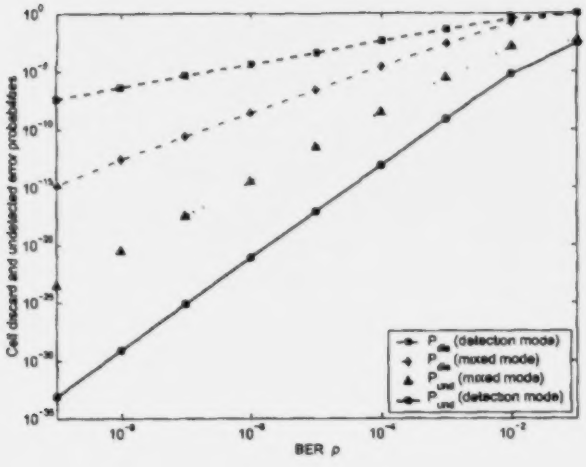

Figure 3: HEC performance in mixed and detection modes.

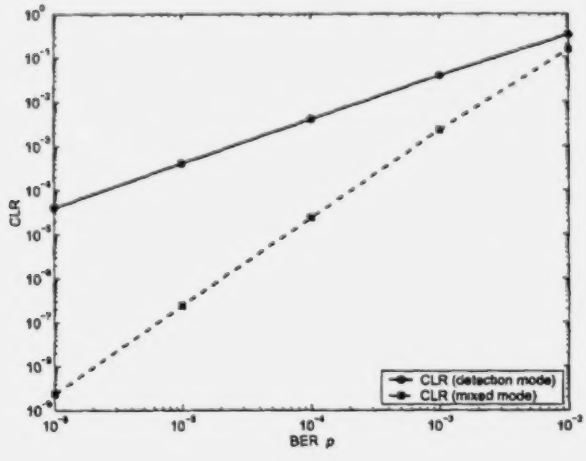

Figure 4: CLR performance in mixed and detection modes.

it is plotted as a function of the BER in Fig. 4 for the two modes of operation. For small values of BER p, the CLR in mixed mode is lower than the CLR in pure detection mode by several orders of magnitude. For fiber-optic links where typically $p \leq 10^{-9}$, the CLR in pure detection mode is less than 10^{-7} and, therefore, sufficiently low to support ATM applications. This explains why the implementation of mixed mode in ATM switches is optional. Furthermore, mixed mode results in a higher probability of undetected header errors than does detection mode, as illustrated in Fig. 3 and, in consequence, in higher Cell Misinsertion Rate (CMR). For BERs in the range of 10^{-6}–10^{-3}, which is typical of wireless links, the CLR ranges from 4×10^{-5} to 3.9×10^{-2} in detection mode and from 2.4×10^{-9} to 2.3×10^{-3} in mixed mode. The CLR performance of the HEC mechanism at BER $p = 10^{-3}$ is inadequate for most ATM applications in both operation modes.

1.3 Cell Delineation

The *Cell Delineation* process of the transmission convergence sublayer is responsible for the identification of cell boundaries in a stream of ATM cells [4].

1.3.1 Cell Delineation Mechanism

Cell delineation is based on the validity of the Header Error Control (HEC) check. If the process finds the correlation between the header bits to be protected (the first 4 bytes of the cell header) and the relevant control bits (the 5th byte of the cell header, which is the HEC field) correct, then it searches for the next header after 48 bytes.

Cell delineation is performed according to the state transition diagram shown in Fig. 5. The

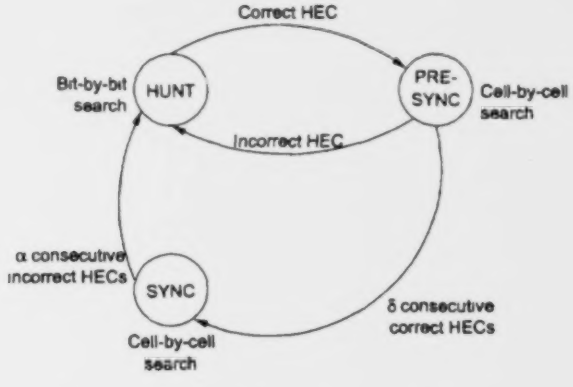

Figure 5: Cell delineation state diagram.

process is in the SYNC state when the receiver is synchronized at cell boundaries. Synchronization is assumed to be lost if an incorrect HEC is obtained α times consecutively. In this case, the process makes a transition from the SYNC to the HUNT state.

In the HUNT state, the delineation process performs a bit-by-bit search for the correct HEC. Once a match has been found, it is assumed that one header has been found and the process makes a transition to the PRESYNC state.

In the PRESYNC state, the process performs a cell-by-cell search for the correct HEC. The process repeats until the correct HEC has been confirmed δ times consecutively, at which point the process moves to the SYNC state. If an incorrect HEC is found, the process returns to the HUNT state.

Cells with correct HECs (or cell headers with single-bit errors which are corrected) that are processed while in the SYNC state are passed to the ATM layer. Any cells received while the process is in the HUNT or PRESYNC state are discarded.

Parameters α and δ are associated with the declaration of loss of synchronization and the declaration of acquisition of synchronization by the cell delineation process, respectively. The larger the value of α, the longer the time required for the process to declare loss of synchroniza-

tion. Similarly, the larger the value of δ, the longer the time required to declare acquisition of synchronization.

The choice of values for α and δ is subject to conflicting performance requirements. More specifically, small values of α will reduce the response time of the cell delineation process in the event of true loss of synchronization, but will also increase the probability of "false" declaration of loss of synchronization, caused inadvertently by transmission errors. In the case of δ, small values will reduce the time required to acquire synchronization at the expense of increasing the probability of falsely declaring synchronization, due to random bit sequences passing the HEC check. The values $\alpha = 7$ and $\delta = 6$ are recommended by ITU-T specification I.432 [4].

1.3.2 Effect of Channel Errors on the Cell Delineation Mechanism

Cell delineation relies on the correctness of ATM cell headers for maintaining and acquiring synchronization; it is therefore impaired by high link-error rates. Errors affect cell delineation by falsely declaring loss of synchronization and by increasing the time required to acquire synchronization. These effects are addressed in the following subsections.

Loss of Cell Synchronization The failure of α consecutive HEC checks, caused by errors in the ATM cell headers, is perceived by the delineation process as loss of synchronization when in fact the receiver is synchronized at cell boundaries. In consequence, the length of time during which the process perceives to be synchronized to the received cell stream decreases in the presence of errors.

The average time spent in the SYNC state before a transition to the HUNT state is forced by bit errors, denoted by T_{sync}, is a measure of the effect of errors on the loss of synchronization. T_{sync} can be easily obtained as a function of the BER, for errors that occur independently, based on the theory of Bernoulli trials. The average number of trials until the first occurrence of m consecutive successes in a sequence of Bernoulli trials with probability of success p_s is given by [5, p. 117]

$$\sum_{i=1}^{m} \left(\frac{1}{p_s}\right)^i = \frac{1 - p_s^m}{(1 - p_s)p_s^m} \quad . \tag{2}$$

Based on the cell delineation algorithm, a transition from the SYNC to the HUNT state takes place whenever α consecutive cells fail the HEC check. The probability of HEC check failure P_f can be expressed in terms of the BER p as

$$\begin{aligned} P_f &= \Pr\{\text{errored cell header}\} \\ &= 1 - (1 - p)^n, \end{aligned}$$

where n is the length of the cell header.

T_{sync}, measured in cell time units, is obtained from Eq. 2 by substituting α for m and P_f for p_s:

$$T_{sync} = \frac{1 - P_f^\alpha}{(1 - P_f)P_f^\alpha} \quad . \tag{3}$$

Results for T_{sync} as a function of p for $\alpha = 7$ are shown in Fig. 6. For $p \leq 10^{-3}$, T_{sync} is dominated by the term $\frac{1}{P_f^\alpha} \approx \frac{1}{(np)^\alpha}$ and, therefore, varies exponentially with $1/p$. For $p = 10^{-3}$, $T_{sync} = 7.28 \times 10^9$ cell time units, the equivalent of 4.82×10^7 seconds or 18.6 months for transmission rate of 64 kb/s. For transmission rate of 2,048 kb/s, T_{sync} is 1.51×10^6 seconds or 17.4 days. Therefore, the performance of the cell delineation process with respect to loss of synchronization is satisfactory for BERs up to 10^{-3} and transmission rates between 64 and 2,048 kb/s. As the BER increases beyond 10^{-3} the performance degrades beyond acceptable levels for the same transmission rate range. For example, for $p = 10^{-2}$, $T_{sync} = 3.43 \times 10^3$ cell time units which translates into 22.73 seconds for 64 kb/s and 0.71 seconds for 2,048 kb/s.

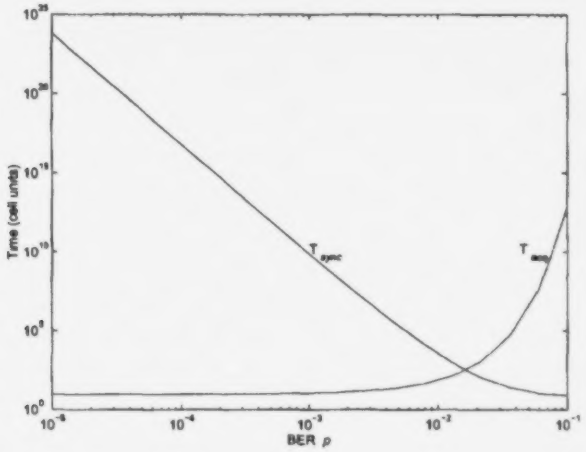

Figure 6: T_{sync} and T_{acq} for the ITU-T recommended cell delineation mechanism.

Acquisition of Cell Synchronization When synchronization is lost, the cell delineation state machine makes a transition to the HUNT state and searches every bit position in the cell for a correct header. A successful HEC check does not necessarily imply that a correct header has been found; a random pattern may match the header with probability $P_s = (1/2)^8$. Synchronization is acquired after δ consecutive correct headers have been confirmed at the same position in the cell in the PRESYNC state. That is, a minimum of $\delta + 1$ header checks—corresponding to, roughly, $\delta + 1$ cell time units—is required to acquire synchronization.

The maximum average synchronization acquisition time, T_{acq}, defined as the average time required for the delineation process to make a transition from the HUNT to the SYNC state when the maximum number of bit positions is tested, can be obtained as a function of the BER, for random errors, from the formula derived in [6]:

$$T_{acq} = \frac{1}{P_c^{\delta+1}} \left\{ (N-1)\frac{P_s}{1-P_s} + \frac{1-P_c^{\delta+1}}{1-P_c} \right\}, \tag{4}$$

where $P_c = (1-p)^n$ is the probability of a header without errors and $N = 424$ is the cell length. T_{acq} is measured in cell time units. Results for T_{acq} as a function of p for $\delta = 6$ are shown in Fig. 6. For $p \leq 10^{-3}$, T_{acq} takes values close to the minimum value of 7 cell time units

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($T_{acq} \leq 10.44$). Thus, the performance of the cell delineation process with respect to acquisition remains satisfactory up to $p = 10^{-3}$. As the value of p increases beyond 10^{-3}, the value of T_{acq} grows rapidly to levels that are unacceptably high. For example, for $p = 10^{-2}$, $T_{acq} = 65.87$ cell time units.

Remark A continuous stream of ATM cells has been assumed in the derivation of T_{sync} (Eq. 3) and T_{acq} (Eq. 4), whereas in practice a frame overhead may interrupt the flow of cells whenever a frame structure is used for cell transport. The Synchronous Optical Network (SONET) and the Plesiochronous Digital Hierarchy (PDH) are examples of frame-based interfaces for ATM cell transport. In the SONET Synchronous Transport Signal Level 1 (STS-1) frame, overhead and payload bytes are transmitted (received) in an alternating fashion; four overhead bytes followed by 86 payload bytes as shown in Fig. 7 [7, p. 329]. Given the relatively low percentage of overhead per frame, the effect of the overhead on T_{sync} and T_{acq} can be ignored.

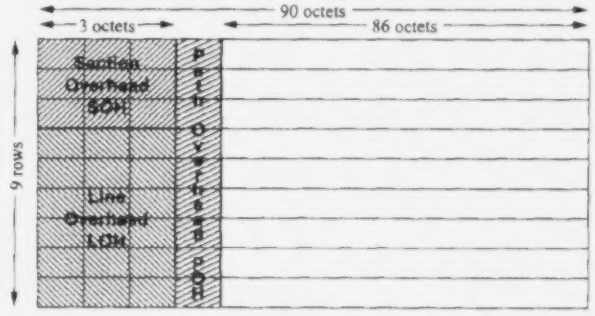

Figure 7: Frame structure for Synchronous Transport Signal Level 1 (STS-1).

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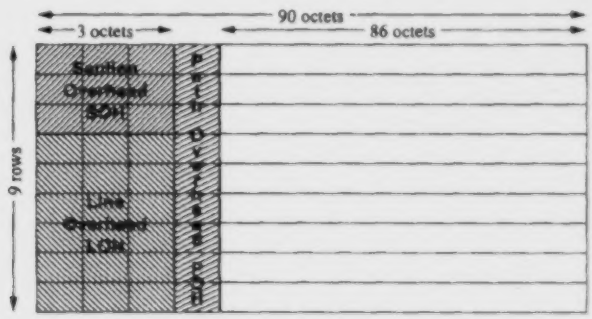


Figure 7: Frame structure for Synchronous Transport Signal Level 1 (STS-1).

2 FEC-Based Error Control for Wireless ATM

2.1 Introduction

From the discussion on the effect of channel errors on the performance of standard ATM in Section 1, it becomes clear that the CLR performance of standard ATM is severely degraded in the presence of wireless-link errors. In consequence, the use of error-control mechanisms is necessary to enable the effective transport of ATM over wireless links and the support of the QoS requirements of the ATM service classes.

Error-control mechanisms applied to communication networks are distinguished in three categories: mechanisms based on Forward Error Correction (FEC), mechanisms based on Automatic Repeat Request (ARQ) and hybrid mechanisms that combine FEC and ARQ. ARQ-based error-control mechanisms may introduce long and unpredictable delays due to retransmissions and are not well-suited for delay-sensitive, constant-bit-rate applications such as voice. This study is focused on the use of FEC for the support of voice services over wireless ATM.

The issue of error control in wireless communication networks is addressed in [8], where alternative general approaches to error control are reviewed and proposals for error control in Wireless ATM are summarized. Some aspects of FEC control in the wireless ATM environment are discussed in [9]. General considerations on the optimization and adaptation of FEC and other error-control algorithms for application to Wireless ATM are also presented in [10].

Error-control mechanisms that have been proposed for the transport of ATM cells over point-to-point wireless links, and which are based on FEC, can be classified into three groups:

a. mechanisms where FEC is applied to the ATM cell stream and all bits are treated identically,

b. mechanisms where FEC is applied independently to the header and payload of the ATM cell and where all cells are treated identically irrespective of the QoS requirements of the connection they belong to, and,

c. mechanisms where FEC is applied independently to the header and payload of the ATM cell and where, moreover, payload FEC is applied on a per Virtual Circuit (VC) basis according to the service class QoS requirements.

The first group includes the Reed-Solomon encoding scheme proposed in the Phase 2 Report of the NATO Project Group 6 (PG/6) [11, 12]. It also includes the concatenated Reed-Solomon/Convolutional code approach adopted in the error-control architecture presented in [2, 13] and considered in [14]. The concatenated RS/convolutional code scheme has been adopted as the baseline FEC algorithm in the Transmission Error Control System of the Survivable ATM architecture [15].

In the first group of mechanisms, header and payload bits in an ATM cell stream are treated identically and protected equally against errors. However, for a given application, the tolerance of the ATM header to errors may differ significantly from the tolerance of the payload. This is true in particular for error-tolerant applications such as voice. The encoding of the cell header and payload by separate codes provides flexibility in choosing the codes that satisfy the application requirements for cell loss and cell errors in the most efficient manner. In contrast,

a mechanism where error correction is applied to the ATM bit stream indiscriminately must satisfy the application requirements on both Cell Loss Ratio and Cell Error Rate and must, therefore, be designed to satisfy the most stringent of the two constraints.

The approach of applying FEC separately to the header and payload has been adopted in the error-control scheme for tactical ATM proposed by GTE Government Systems [16, 17]. The same principle is the basis for the approach presented in [18, 19], although the work is not intended specifically for tactical ATM.

The error-control approach proposed for tactical ATM by the Defence Evaluation and Research Agency (DERA) [20, 21] is different from the above in that it recommends applying FEC to the ATM bit stream (channel encoding) as well as increasing header protection by duplicating the header of the standard ATM cell for transmission over the wireless link.

In the second group of mechanisms, encoding is applied to every cell in the stream of multiplexed ATM connections in an identical manner at the TC sublayer. In standard ATM, cells belonging to different ATM connections are not distinguishable at the TC sublayer. Consequently, error control cannot be applied on the basis of the QoS requirements of the individual service classes but rather has to be performed on the basis of the least error-tolerant service class using the link. Applications with less stringent requirements will be protected with encoding schemes more powerful than necessary with the potential of wasted bandwidth. Alternatively, FEC can be applied to the ATM cell payload on a per-VC basis at the AAL layer [22, 23, 24].

The performance of the error-control mechanisms for ATM transport over wireless point-to-point links proposed by the NATO PG/6 group, NTT and DERA is addressed in the following.

2.2 NATO PG/6 Proposal

2.2.1 System Description

The NATO PG/6 group has proposed a simple FEC scheme based on Reed-Solomon codes for the TACOMS Post-2000 project [11, 12]. In the proposed scheme, the standard ATM cell is encoded using a (59,53) shortened RS code defined over GF(2^8) (Fig. 8). The code has

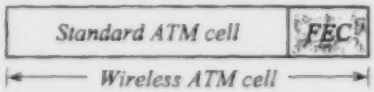


Figure 8: Block structure of wireless ATM cell for the PG/6 proposal.

error-correcting capability $t = 3$ bytes and code rate $r = 0.90$.

In the following subsection it is shown that the code achieves CLR $\leq 1.3 \times 10^{-3}$ and Residual BER $p_{res,b} \leq 8 \times 10^{-5}$ for BER $p \leq 10^{-3}$ over the random-error (Additive White Gaussian Noise - AWGN) channel.

2.2.2 Performance Over the Random-Error Channel

Given an (n,k) RS code with m-bit symbols and symbol-correcting capability t and considering bounded-distance decoding, the probability of incorrect decoding of a received codeword is given by the probability that the number of errored codeword symbols exceeds t [25, p. 219]:

$$p_w = \sum_{j=t+1}^{n} \binom{n}{j} p_s^j (1-p_s)^{n-j} = 1 - \sum_{j=0}^{t} \binom{n}{j} p_s^j (1-p_s)^{n-j}. \tag{5}$$

Probability p_s denotes the symbol-error probability and is given by:

$$p_s = \sum_{j=1}^{m} \binom{m}{j} p^j (1-p)^{m-j} = 1 - (1-p)^m,$$

for m-bit symbols and random-error channel BER p. The quantity p_w includes contributions due both to undetected and detected errors.

Under the assumption that all incorrect decoding events result in codeword (cell) discard, the probability of incorrect decoding p_w is equal to the CLR. Therefore, p_w is an upper bound for CLR.

Results for p_w for shortened RS codes defined over GF(2^8) with $k = 53$ information symbols (the size of an ATM cell), derived by means of Eq. 5, are shown in Fig. 9(a) for different values of code error-correction capability t ($1 \leq t \leq 6$).

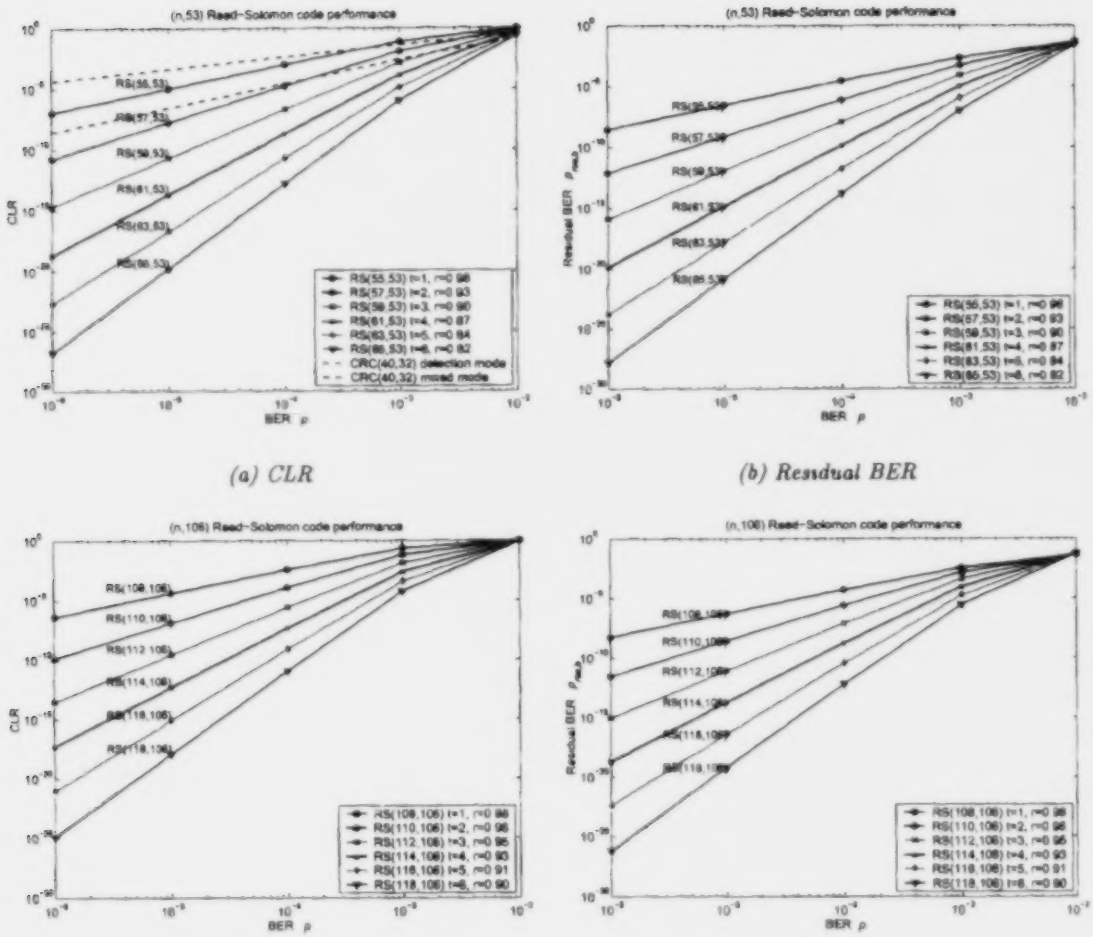
The residual BER (or post-decoding bit-error probability) bounded by [25, p. 333]:

$$p_{res,w} = \frac{2^{m-1}}{2^m - 1} \sum_{j=t+1}^{n} \frac{j+t}{n} \binom{n}{j} p_s^j (1-p_s)^{n-j}, \tag{6}$$

can also be useful in evaluating the performance of the proposed scheme. The residual BER cannot be directly associated with performance measures of interest like the payload bit-error rate by analytical means. However, it is expected in general that the lower the value of $p_{res,b}$, the better the performance of the encoding scheme. Results for $p_{res,b}$ are shown in Fig. 9(b). Note that for random BER $p = 10^{-3}$, the (59,53) RS code achieves CLR $= 1.3 \times 10^{-3}$ and $p_{res,b} = 7.8 \times 10^{-5}$. The CLR achieved by this encoding scheme for $p = 10^{-3}$ is almost the same as the CLR achieved by using traditional HEC in mixed mode (2.3×10^{-3}).

The CLR and residual BER performance for $p \leq 10^{-3}$ will improve by increasing the number of information symbols per codeword from $k = 53$ to $k = 106$ (two ATM cells per codeword) and maintaining the same code rate $r = 0.90$ as illustrated by the results of Figs. 9(c) and 9(d), respectively. In this case, the CLR is given by $CLR = 2p_w$, since the discard of a single codeword results in the discard of two successive ATM cells. More specifically, the (118,106) code with rate $r = 0.90$ and $t = 6$ symbols achieves, for $p = 10^{-3}$, CLR $= 5 \times 10^{-5}$ and $p_{res,b} = 2.8 \times 10^{-6}$ compared to 1.3×10^{-3} and 7.8×10^{-5}, respectively, achieved by the (59,53) code. This performance improvement is achieved at the expense of increased encoding delay introduced by the processing of ATM cells in pairs.

For completeness, the performance of the (59,53) RS code is compared to that of shortened BCH codes from the class of original BCH codes with block size equal to 511. For an (n,k) BCH



(a) CLR *(b) Residual BER*

(c) CLR *(d) Residual BER*

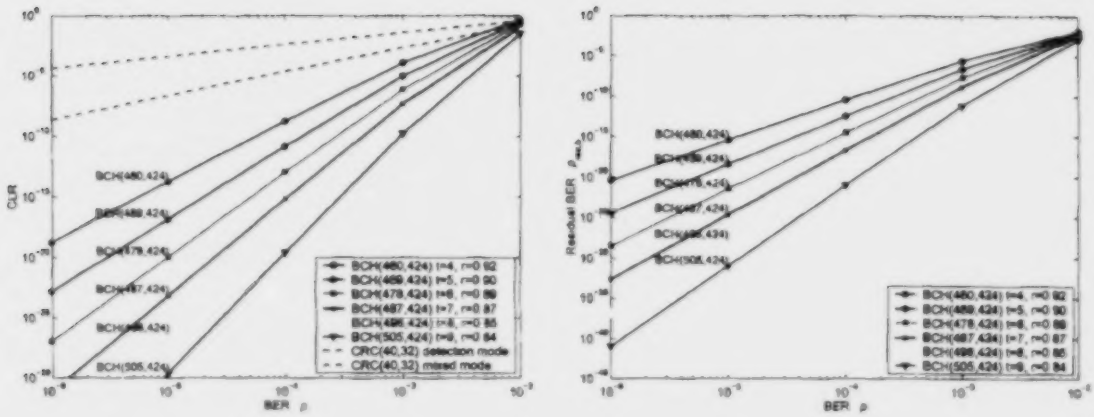
Figure 9: PG/6 error-control scheme performance.

code, p_w and $p_{res,b}$ are obtained from Eqs. 5 and 6, respectively, for $m = 1$. Results for the two quantities for different values of bit-error-correcting capability t are shown in Fig. 10.

Note that for $p = 10^{-3}$ the (469,424) BCH code with rate $r = 0.90$ and $t = 5$-bit error-correcting capability outperforms both the (59,53) RS code and the (118,106) RS code by achieving CLR $= 9.6 \times 10^{-6}$ and $p_{res,b} = 2.1 \times 10^{-7}$. For $p = 10^{-5}$, the (59,53) RS code is outperformed by the BCH code, which in turn is outperformed by the (118,106) RS code. These performance comparison results are tabulated in Table 1.

Furthermore, the (487,424) BCH code ($r = 0.87$, $t = 7$) achieves CLR $\leq 4.84 \times 10^{-8}$ and $p_{res} < 1.5 \times 10^{-9}$ for $p \leq 10^{-3}$.

Remarks The (469,424) BCH code outperforms the (59,53) RS code of equal code rate $r = 0.90$ over the random-error rates of interest ($10^{-6} \leq p \leq 10^{-3}$). It should be pointed out,



(a) CLR *(b) Residual BER*

Figure 10: BCH code performance.

Code		rate	t (symbols)	Channel	BER (p)	CLR	$p_{res,b}$
RS	(59,53)	0.90	3	AWGN	10^{-3}	1.3×10^{-3}	7.8×10^{-5}
RS	(118,106)	0.90	6	AWGN	10^{-3}	5.0×10^{-5}	2.8×10^{-6}
BCH	(469,424)	0.90	5	AWGN	10^{-3}	9.6×10^{-6}	2.1×10^{-7}
RS	(59,53)	0.90	3	AWGN	10^{-5}	1.9×10^{-11}	1.1×10^{-12}
RS	(118,106)	0.90	6	AWGN	10^{-5}	1.1×10^{-18}	6.1×10^{-20}
BCH	(469,424)	0.90	5	AWGN	10^{-5}	1.4×10^{-17}	3.3×10^{-19}

Table 1: Block code performance.

however, that in the burst-error environment RS codes have the advantage of being inherently resistant to burst errors of length less than or equal to the symbol size.

2.3 NTT Proposal

2.3.1 System Description

In the approach presented in [19], BCH codes are considered for header and payload error control. A wireless ATM cell for transmission over the radio link is formed from the standard ATM cell by removing the HEC byte and replacing it with the parity-check bits of a BCH code stronger than the 8-bit HEC CRC. Moreover, the parity-check bits used for the protection of the payload are appended to the standard cell. The structure of the wireless ATM cell for this proposal is illustrated in Fig. 11; fields FEC_0 and FEC_1 indicate the parity-check bits for the header and payload codes, respectively. At the receiving end, the wireless ATM cell header

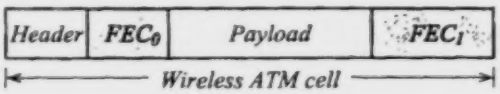


Figure 11: Block structure of wireless ATM cell for the NTT proposal.

is checked for correctness. Wireless ATM cells with detected uncorrectable header errors are discarded, while cells with no detected header errors are reverted to standard ATM cells by removing the header parity-check bits and reintroducing the HEC byte as well as decoding the payload FEC. Note that an undetected error in the ATM cell header will result in cell misrouting and, eventually, in cell discarding.

The performance of the NTT proposal with respect to the CLR and the Residual BER over the random-error channel are investigated in the following subsection.

2.3.2 Performance Over the Random-Error Channel

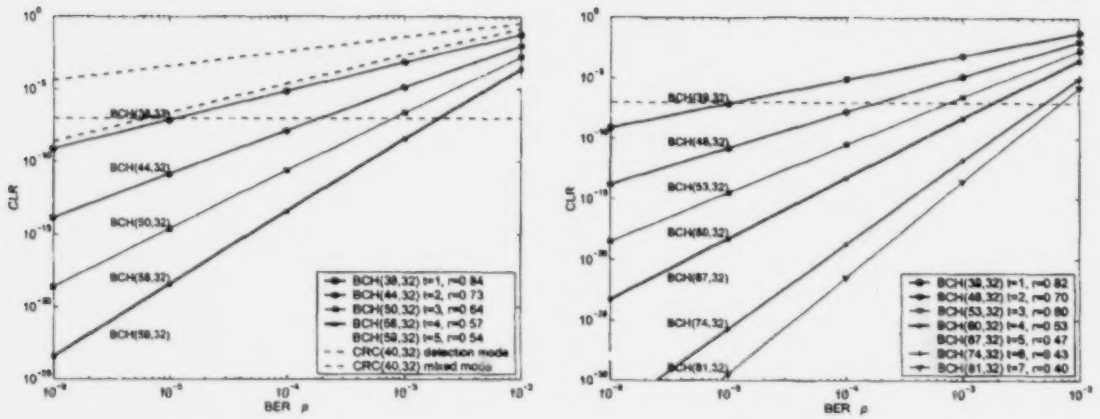
Header BCH Code The CLR performance of the scheme is determined by the probability of incorrect codeword decoding for the header BCH code, given by Eq. 5 for $m = 1$:

$$p_w = \sum_{i=t+1}^{n} \binom{n}{i} p^i (1-p)^{n-i},$$

where t is the bit-error-correcting capability and n the block size of the code.

CLR results for shortened BCH codes obtained from the original codes of block size 63 bits are shown in Fig. 12(a) for different values of t ($1 \leq t \leq 5$).

The (56,32) code with $t = 4$ and the (59,32) code with $t = 5$ achieve CLR $< 10^{-7}$ for $p \leq 10^{-3}$. The $(63-\ell,k-\ell)$ shortened BCH codes from the class of original (63,k) BCH codes, where $k - \ell = 32$, can provide error-correcting capability t of up to 5 bits only. Shortened BCH codes with error-correcting capability higher than 5 bits and up to 15 bits, must be sought from the class of (127,k) codes. CLR results for some of these codes ($1 \leq t \leq 7$) are shown in Fig. 12(b). For $t \leq 5$, the codes from the (63,k) class achieve CLR values that are slightly better (within the same order of magnitude) than those obtained from the (127,k) class for the same value of t. In addition, the former are more efficient than the latter as they are higher rate codes. Unless the desired CLR value over the random-error channel is less than 10^{-11} for



(a) BCH (63,n) codes *(b) BCH (127,n) codes*

Figure 12: Header BCH code CLR performance.

$p \leq 10^{-3}$ (or less than 10^{-5} for $p \leq 10^{-2}$), it is preferable to use codes of the (63,k) class. These points become evident from the performance results of Table 2.

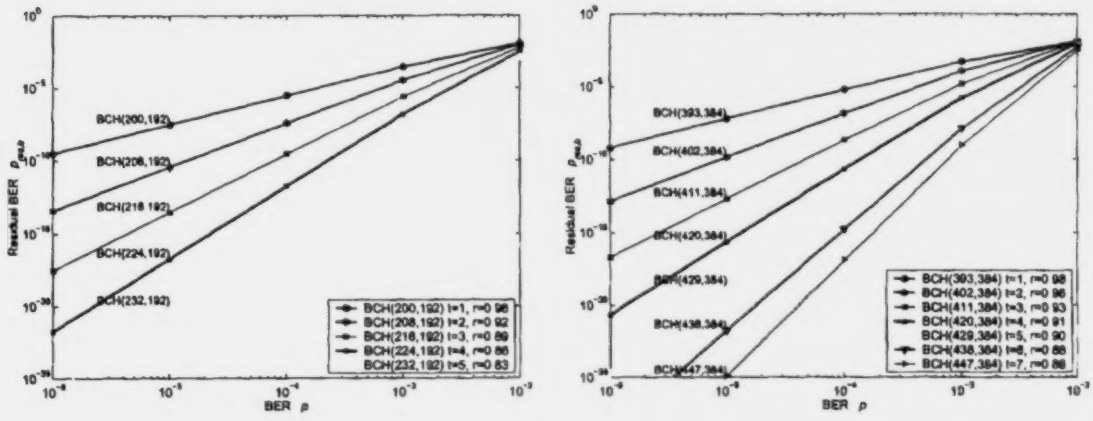
Code		rate	t (symbols)	Channel	BER (p)	CLR
BCH	(44,32)	0.73	2	AWGN	10^{-3}	1.3×10^{-5}
BCH	(50,32)	0.64	3	AWGN	10^{-3}	2.2×10^{-7}
BCH	(56,32)	0.57	4	AWGN	10^{-3}	3.7×10^{-9}
BCH	(59,32)	0.54	5	AWGN	10^{-3}	4.3×10^{-11}
BCH	(46,32)	0.70	2	AWGN	10^{-3}	1.5×10^{-5}
BCH	(53,32)	0.60	3	AWGN	10^{-3}	2.8×10^{-7}
BCH	(60,32)	0.53	4	AWGN	10^{-3}	5.2×10^{-9}
BCH	(67,32)	0.47	5	AWGN	10^{-3}	9.5×10^{-11}
BCH	(74,32)	0.43	6	AWGN	10^{-3}	1.7×10^{-12}
BCH	(81,32)	0.40	7	AWGN	10^{-3}	3.0×10^{-14}

Table 2: Header BCH code performance.

Payload BCH Code The payload BER performance of the scheme is given by the residual BER of the payload BCH code, obtained from Eq. 6 for $m = 1$:

$$p_{res,b} = \sum_{j=t+1}^{n} \frac{j+t}{n} \binom{n}{j} p^j (1-p)^{n-j}. \tag{7}$$

The NTT approach recommends breaking the payload into two segments of 192 bits each and applying the same BCH code of appropriate error-correcting capability t to each segment. The codes under consideration are obtained from the class of BCH codes with block size equal to 255 through shortening; results for the residual BER for different values of t are shown in



(a) BCH (255,n) codes *(b) BCH (511,n) codes*

Figure 13: Payload BCH code Residual BER performance.

Fig. 13(a). The (224,192) BCH code with $t = 4$ and all the codes from the same class with higher error-correcting capability achieve residual BER $\leq 10^{-6}$ for $p \leq 10^{-3}$.

For $p \leq 10^{-3}$ and the same code rate r, better residual BER values are achieved when the 384 payload bits are encoded in a single codeword by using shortened BCH codes from the original class with block size 511, as illustrated by the results in Fig. 13 and Table 3.

A residual BER value of less than 10^{-6} is obtained for $p \leq 10^{-3}$ by applying the (224,192) BCH code with $t = 4$ or the (429,384) BCH code with $t = 5$ and the higher error-correcting capability codes.

Code		rate	t (symbols)	Channel	BER (p)	$p_{res,b}$
BCH	(200,192)	0.96	1	AWGN	10^{-3}	2.7×10^{-4}
BCH	(208,192)	0.92	2	AWGN	10^{-3}	3.1×10^{-5}
BCH	(216,192)	0.89	3	AWGN	10^{-3}	2.4×10^{-6}
BCH	(224,192)	0.86	4	AWGN	10^{-3}	1.5×10^{-7}
BCH	(402,384)	0.96	2	AWGN	10^{-3}	1.0×10^{-4}
BCH	(411,384)	0.93	3	AWGN	10^{-3}	1.5×10^{-5}
BCH	(420,384)	0.91	4	AWGN	10^{-3}	1.6×10^{-6}
BCH	(429,384)	0.90	5	AWGN	10^{-3}	1.5×10^{-7}
BCH	(438,384)	0.88	6	AWGN	10^{-3}	1.2×10^{-8}
BCH	(447,384)	0.86	7	AWGN	10^{-3}	8.5×10^{-10}

Table 3: Payload BCH code performance.

The combination of the (56,32) BCH code for the header and the (224,192) BCH code for the payload, satisfies the constraints CLR $\leq 10^{-7}$ and Residual BER $\leq 10^{-6}$ for $p \leq 10^{-3}$ over the random-error channel. The total overhead required due to coding is 88 bits, resulting in a code rate $r = 416/504 = 0.83$ for the entire cell. The combination of the (56,32) BCH code and

Header Code	Payload Code	Parity bits	Coding rate	Channel	BER (p)	CLR	$p_{res,b}$
BCH (56,32)	BCH (224,192)	88	0.83	AWGN	10^{-3}	3.7×10^{-9}	1.5×10^{-7}
BCH (56,32)	BCH (429,384)	69	0.86	AWGN	10^{-3}	3.7×10^{-9}	1.5×10^{-7}
BCH (56,32)	BCH (224,192)	88	0.83	AWGN	10^{-5}	3.8×10^{-19}	1.8×10^{-17}
BCH (56,32)	BCH (429,384)	69	0.86	AWGN	10^{-5}	3.8×10^{-19}	2.1×10^{-19}

Table 4: Separate header and payload encoding – BCH code performance.

the (429,384) BCH code for the payload meets the same constraints with a slightly higher code rate $r = 416/485 = 0.86$ (Table 4). Therefore, the latter combination has a slight advantage with respect to bandwidth utilization efficiency of the random-error channel.

Remarks

- The combination of the (56,32) BCH code for the header and the (429,384) BCH code for the payload with code rate $r = 0.86$ satisfies the constraints CLR $\leq 10^{-7}$ and Residual BER $\leq 10^{-6}$ for $p \leq 10^{-3}$ over the random-error channel.
- The combination of the (56,32) BCH code for the header and the (224,192) BCH code for the payload with code rate $r = 0.83$ satisfies the constraints CLR $\leq 10^{-7}$ and Residual BER $\leq 10^{-6}$ for $p \leq 10^{-3}$ over the random-error channel.

2.4 DERA Proposal

2.4.1 System Description

An approach based on a Link Hardening Appliqué (LHA), that sits between a Commercial-Off-The-Shelf (COTS) ATM switch and a radio modem, has been adopted by (DERA) [20]. The purpose of the LHA is to interface to a standard ATM switch and suitably process the ATM cell stream. The processing of a standard ATM cell by the LHA at the transmitting end results in a "hardened" wireless ATM cell which is passed to a radio modem for transmission across the error-prone link (Fig. 14). The LHA at the receiving end is responsible for error recovery and for reproducing a cell with standard ATM structure from the wireless ATM cell and passing it on to the wired network. The function of the LHA is to protect ATM mechanisms against the

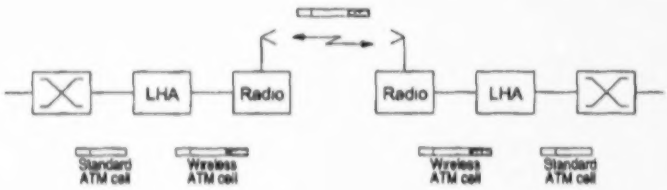


Figure 14: DERA link hardening scheme.

high radio-link error rates and so should be distinguished from that of a modem which merely improves the radio-link error rates to very low values comparable to those of fiber-optic links.

The structure of the wireless ATM cell is shown in Fig. 15. In this approach, the error control applied to ATM cells for protection of voice transmissions includes the use of a duplicate cell header as well as optional FEC control [21]. Note that the second cell header is placed after

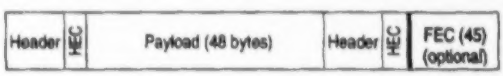


Figure 15: Wireless ATM cell structure proposed for voice transmissions.

the payload, and is separated from the FEC field of length 45 by two bits. FEC is applied to the entire standard ATM cell including the duplicate cell header.

The performance of this approach when FEC is applied in addition to the duplicate header cannot be evaluated by using analytical means. The effect of the combined use of FEC and duplicate HEC check on the performance of the scheme, while of interest due to the concatenation of codes, must be addressed through simulation.

2.4.2 Performance Over the Random-Error Channel

The performance of the duplicate-header scheme in terms of CLR when FEC is not applied can be easily determined from the performance of the HEC mechanism (Section 1.2.2).

The performance of the scheme is investigated for two cases:

(a) header-error detection without error correction, and,

(b) header-error detection and single-bit error correction.

(a) Header-Error Detection

When header-error correction is not performed, the cell discard and undetected error probabilities for the duplicate-header scheme, denoted by P_{dis}^{dup} and P_{und}^{dup} respectively, can be easily derived in terms of the respective probabilities for the traditional single header HEC scheme in detection mode, P_{dis} and P_{und} (Appendix A).

Under the assumptions that:

a) a cell is discarded whenever both cell headers have detected errors, and,

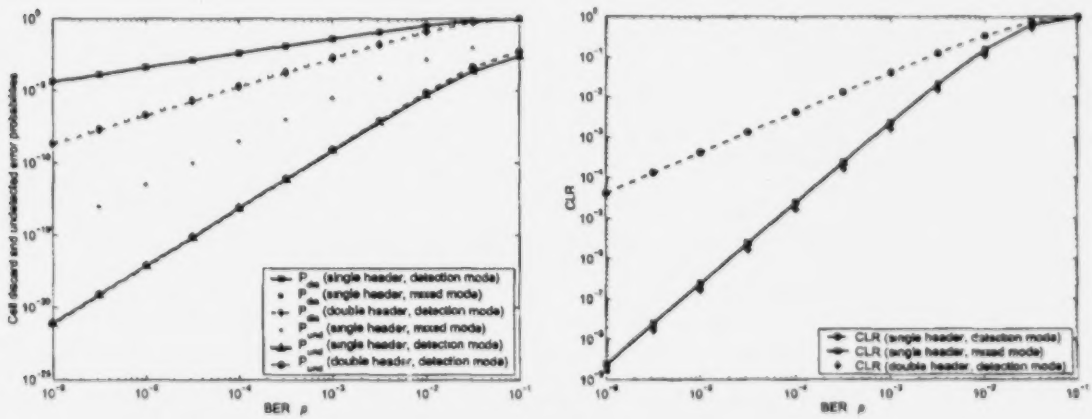
b) when no errors are detected in any of the two headers, one of the headers is removed in a random fashion,

P_{dis}^{dup} and P_{und}^{dup} are given by:

$$P_{dis}^{dup} = P_{dis}^2, \tag{8}$$

$$P_{und}^{dup} = P_{und}(1 + P_{dis}). \tag{9}$$

Results for both quantities are shown in Fig. 16(a). The cell header duplication results in cell discard probability that is approximately the same to that achieved by the single-header scheme in mixed mode. Furthermore, it results in undetected error probability that is almost identical to that achieved by the single-header scheme in detection mode. Therefore, cell header duplication has a clear advantage over the single header scheme in both detection and mixed operation modes at the expense of increased overhead.



(a) Cell discard and undetected error performance *(b) CLR performance*

Figure 16: Duplicate-header scheme performance - Header-error detection case.

The CLR performance under the duplicate-header scheme, $\text{CLR}^{dup} = P_{dis}^{dup} + P_{und}^{dup}$, is compared to the CLR performance under the traditional HEC mechanism in Fig. 16(b). The

duplicate-header scheme achieves slightly improved performance compared to that of the single-header scheme in mixed mode. For $p \leq 10^{-3}$, a CLR value of less than 1.5×10^{-3} is achieved.

(b) Header-Error Correction

When the single-bit error-correcting capability of the HEC CRC code is applied, the cell discard probability, $(P_{dis}^{dup})'$, and the undetected error probability, $(P_{und}^{dup})'$, are derived in terms of the probabilities of detected and undetected header error events in correction mode, denoted by P'_{dis} and P'_{und} (Appendix A), respectively:

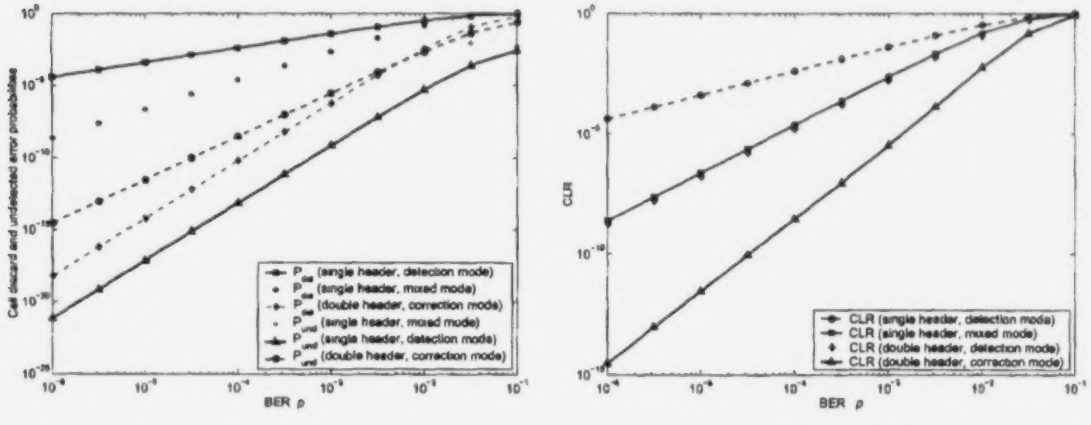
$$(P_{dis}^{dup})' = (P'_{dis})^2 \tag{10}$$

$$(P_{und}^{dup})' = P'_{und}(1 + P'_{dis}). \tag{11}$$

In correction mode, the probability of a detected error event P'_{dis} decreases compared to P_{dis} in detection mode due to single-bit-error correction, $P'_{dis} < P_{dis}$. Furthermore, the undetected error probability P'_{und} increases compared to P_{und}, due to incorrect correction of multiple-bit errors, $P'_{und} > P_{und}$. In consequence, header-error correction results in improved cell discard probability compared to case (a) where only header-error detection is applied:

$$(P_{dis}^{dup})' = (P'_{dis})^2 < P_{dis}^2 = P_{dis}^{dup}. \tag{12}$$

On the other hand, the undetected error probability $(P_{und}^{dup})'$ increases compared to P_{und}^{dup}. More specifically, the duplicate-header scheme with header-error correction has the highest undetected error probability amongst the single-header and duplicate-header schemes. In addition, it is the only scheme with cell discard probability lower than the undetected error probability (except for high channel-error rates $p > 10^{-3}$), resulting in more cells being misrouted than discarded. For example, for $p = 10^{-3}$, $(P_{und}^{dup})' = 2.8 \times 10^{-6}$ and $(P_{dis}^{dup})' = 5.7 \times 10^{-7}$. These observations can be verified from the results for $(P_{dis}^{dup})'$ and $(P_{und}^{dup})'$ shown in Fig. 17(a).


Cell discard and undetected error probabilities
BER p
P_dis (single header, detection mode)
P_dis (single header, mixed mode)
P_dis (double header, correction mode)
P_und (single header, mixed mode)
P_und (single header, detection mode)
P_und (double header, correction mode)
CLR
BER p
CLR (single header, detection mode)
CLR (single header, mixed mode)
CLR (double header, detection mode)
CLR (double header, correction mode)

(a) Cell discard and undetected error performance *(b) CLR performance*

Figure 17: Duplicate-header scheme performance – Header-error correction case.

The cell discard probability in this case is significantly lower than the cell discard probability when no error correction is attempted (Figs. 16(a), 17(a)). At the same time, the probability of

undetected error for this range of BERs is almost identical to that obtained if a single header is used in mixed mode. It is this quantity $(P_{und}^{dup})'$ that dominates the Cell Loss Ratio results shown in Fig. 17(b).

Nevertheless, the CLR is lower than the CLR obtained when no error correction is applied by at least three orders of magnitude for $p \leq 10^{-3}$. For $p \leq 10^{-3}$, a CLR value of less than 3.4×10^{-6} is achieved. Even though the duplicate-header scheme with header-error correction provides for low CLR values, it is considered ineffective due to the high undetected error rates.

3 Approaches for Adapting ATM to the Wireless Medium

The error-control mechanisms discussed in Section 2 address the protection of the ATM cell against errors by using FEC without consideration to the effect of errors on the Wireless ATM frame/cell synchronization processes.

The two approaches presented in this section propose complete solutions for the transport of ATM cells over point-to-point wireless transmission links.

3.1 Yurie Approach

A solution for the adaptation of ATM to low-speed, error-prone environments has been developed by Yurie Systems (acquired by Lucent Technologies in May 1998) and implemented in the ATM access concentrators LDR100 and LDR200 (predecessors to Lucent's PacketStar Access Concentrators 60 and 120, respectively). The solution is based on a multi-layered error-correction approach with key features [22]:

- LANET, a physical layer protocol with enhanced cell delineation capabilities,
- an error-tolerant addressing scheme to enhance header protection against errors, and,
- application-dependent payload encoding on a per-virtual-circuit basis at the Service Specific Convergence Sublayer (SSCS) of the ATM Adapatation Layer (AAL).

3.1.1 LANET Frame Structure

LANET uses a frame-based transmission format with frame structure as shown in Fig. 18 [23]. The frame has length 2400 bytes and includes 45 ATM cells, a total of 2385 bytes, and

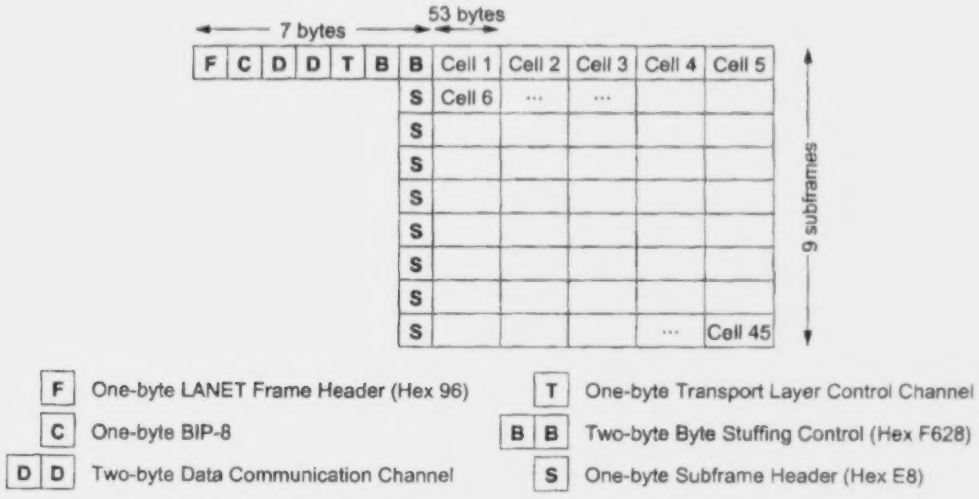


Figure 18: LANET frame structure.

15 bytes of overhead which accounts for 0.625% of the transmission bandwidth. ATM cells are accommodated in nine subframes, each of which carries five ATM cells as shown in Fig. 18. The first LANET subframe starts with a one-byte frame header field **F** followed by a one-byte bit interleaved parity (BIP-8) field **C**, where the checksum is computed over the previous frame, excluding the frame header. A two-byte Data Communication Channel field **DD** is used to provide for the operation, administration and maintenance of the communication link. A single-byte field **T** is reserved for the Transport Layer Control Channel. A two-byte field **BB** has been included for the purpose of byte-stuffing control and has been assigned the hexadecimal value F628. In the rest of the subframes, ATM cells are preceded by identical single-byte subframe headers **S** with hexadecimal value E8.

3.1.2 Cell Delineation Mechanism

The LANET framing (frame and subframe) headers are used in conjunction with traditional HEC to enhance the performance of the ITU-T recommended cell delineation algorithm (Section 1.3) with respect to T_{sync} and T_{acq} in error-prone environments. In addition to using the framing headers for maintaining and acquiring synchronization, the process uses a data "history" buffer for reducing the synchronization acquisition time.

A simple state machine diagram for the mechanism is shown in Fig. 19. The timely arrival

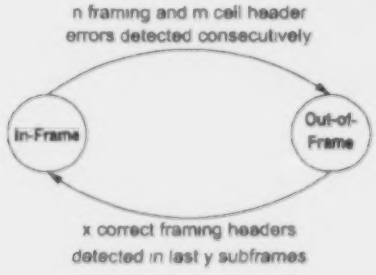
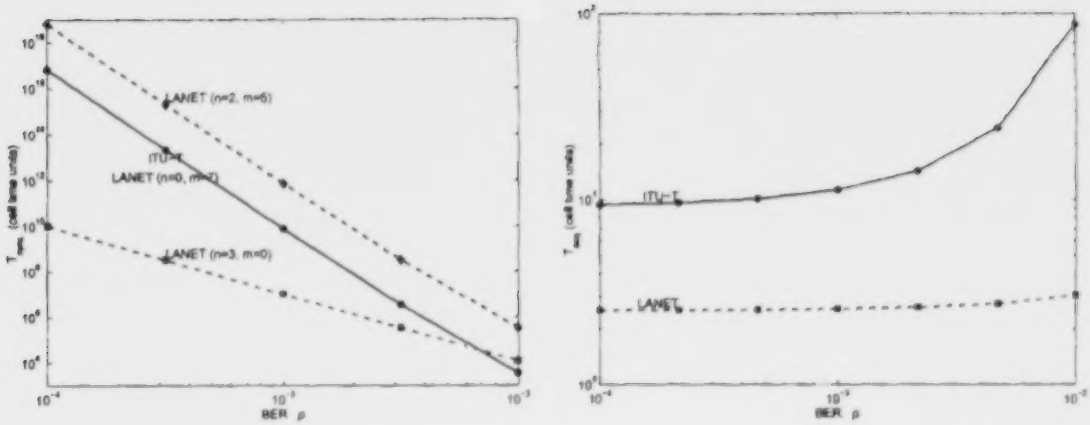


Figure 19: LANET cell delineation state diagram.

of the LANET framing header patterns is used as a confidence check, confirming that the system is properly synchronized. Loss of synchronization is declared when n framing header errors and m cell header errors are consecutively detected at the receiver, causing a transition from the In-Frame to the Out-of-Frame state. For $n = 0$ and $m = 7$ the out-of-frame detection process behaves the same as the process for detecting loss of cell synchronization used by the ITU-T recommended cell delineation process (Section 1.3.1).

The performance of the process with respect to T_{sync}, where T_{sync} is the mean time spent in the In-Frame state, for three sets of values for parameters m, n are shown in Fig. 20(a). Note that the value of T_{sync} for $n = 2$, $m = 5$, is approximately two orders of magnitude higher than its value for $n = 0$, $m = 7$, obtained for the standard ATM cell delineation method, which is based on the correctness of cell headers only. The cell delineation process used by LANET improves performance by taking advantage of the fact that short framing headers are less likely to be errored compared to the considerably longer ATM cell headers. As the BER p approaches the value 10^{-2}, T_{sync} takes values that are too low to support any practicl application. For



(a) T_{sync} *(b)* T_{acq}

Figure 20: LANET cell delineation algorithm performance.

example, for $p = 10^{-2}$, T_{sync} is in the order of minutes only for transmission rates as low as $r = 64$ kb/s.

The process declares acquisition of synchronization when x correct framing headers are identified in the last y subframes of past data (the history buffer is assumed to hold at least y subframes of data). More specifically, the process performs a bit-by-bit backward search for a correct subframe in the buffer and, when this is found, it continues searching for $(x-1)$-out-of-x correct framing headers. The parameter settings $x = 3$, $y = 4$ have been used in implementations of the process. Results for the mean synchronization acquisition time T_{acq}, as derived in [22], are presented in Fig. 20(b).

The process for acquiring cell synchronization used by the LANET cell delineation mechanism relies on the correctness of the framing headers only, rather than on the correctness of ATM cell headers as is the case with the ITU-T recommended cell delineation algorithm. The periodic occurrence of predictable framing header patterns, which are short enough to have a reasonable chance of surviving errors, allows for the quick sorting of the data stored in the history buffer. This results in the significant reduction of T_{acq} compared to standard ATM cell delineation, especially as the BER approaches 10^{-2}, as shown in Fig. 20(b).

3.1.3 Multiple Redundancy Addressing

A nontraditional approach has been implemented for the protection of the cell header and, more specifically, the header VPI/VCI fields, against errors. In this approach, multiple virtual circuits are established to the same destination. The addresses for the circuits are within the error space of the principal address used for the actual transmission. Thus, the most probable error patterns occurring in the address field will simply change the address to another valid one. In practice, tolerance of 2-bit random errors or 5-bit burst errors requires setting up $N = 526$

addresses[2] per virtual channel [22]. This implementation requires no special hardware and no modifications to the current standard. It encodes the header address within the same 40-bit header space of standard ATM cells, as opposed to header error protection schemes based on error correction. The latter may require additional header space to accommodate parity-check bits and may introduce delay due to encoding.

Due to the addressing redundancy, this scheme limits the number of users that can be supported. This is not considered a serious constraint in the wireless environment where the links will likely be used to support a small number of users due to bandwidth limitations. A serious drawback of this approach is that the address of the signaling channel, VPI=0, VCI=5, is within 2 bit errors of the idle cell address VPI=0, VCI=0; therefore, signaling will be inhibited in high-error conditions. It must also be noted that the approach does not protect the GFC, PTI and CLP fields of the header, which need to be separately protected with the payload.

3.1.4 Payload Encoding

The approach developed by Yurie provides the flexibility of using application-dependent payload error correction schemes depending on the error tolerance of the application at the SSCS.

3.1.5 Comments

Test results reported by Yurie claim that the combination of LANET, the 2-bit random/5-bit burst-error-tolerant addressing scheme and a software Reed-Solomon (9 bytes into 15 bytes) encoded payload can reliably transmit ATM cells over a noisy medium at random BER up to 10^{-3} and 5-bit burst errors at BER up to 10^{-2}.

[2]The size of the address field is 24 bits, that is, the size of the VPI/VCI fields at the UNI. The number of addresses N that must be set up in addition to the principal address, is given by the number of 2-bit random-error patterns in a sequence of 24 bits, N_r, and the number of error patterns with one or more (up to four) 5-bit burst errors, N_b: $N = N_r + N_b$. There are $N_r = \binom{24}{2} = 276$ error patterns of weight 2 in a sequence of 24 bits. N_b can be expressed as $N_b = N_1 + N_2 + N_3 + N_4$, where N_i is the number of error patterns with i 5-bit error bursts. By use of combinatorics, it can be shown that $N_1 = 20$, $N_2 = 105$, $N_3 = 120$, $N_4 = 5$, and thus, $N_b = 250$ and $N = N_r + N_b = 526$.

3.2 GTE Tactical ATM

An approach for ATM transmission over tactical communication links and, in particular, US Army LOS microwave links, has been developed by GTE Government Systems Corporation. The design provides distinct solutions for voice and data; the solution applied to data uses the solution proposed for voice enhanced by payload error-control encoding.

3.2.1 Wireless Environment/System Characteristics

The approach has been developed for LOS microwave links, the most prevalent links used for tactical communications. The data rates supported by these tactical links include 256, 512, 1024 and 2048 kb/s. The links are characterized by long-term average bit-error rates in the range of 10^{-6} 10^{-3}.

Tactical LOS microwave links can sometimes be accurately characterized as AWGN channels, when the terrain between the receiver and the transmitter does not support signal reflections and all received energy is associated with the direct path. When there is a significant amount of reflected energy in addition to the direct path, tactical LOS links are characterized as slow Rician fading channels [17].

Both the AWGN and Rician fading channel models have been used for the performance evaluation of the design. The parameters $K = 20$ dB and $K = 10$ dB have been considered for the Rician channel model, where K is the ratio of the energy received along the direct path to the total reflected energy. The $K = 20$ dB model is considered the most representative channel model and the $K = 10$ dB model the worst-case model.

Furthermore, the design assumes binary Frequency-Shift-Keying (FSK) modulation with noncoherent detection and hard-decision decoding, which is implemented in the tactical radios of interest to the GTE work, and the choice of error-control codes has been based on this assumption.

3.2.2 Key Features

The key features of the error-control approach for ATM transmission over tactical communication links presented in [16] are:

- BCH error-control coding is applied for header error control of both voice and data transmissions.
- BCH error-control coding is applied for payload-error control of data transmissions. Payload error-control coding is applied in the case of data transmissions in order to limit the number of retransmissions required by traditional ARQ at the Transport Layer.
- Information is transported in tactical ATM frames, where each frame is associated with a single standard ATM cell.

3.2.3 Tactical ATM Frame Structure

The transmission format used for the transport of ATM cells is different from the frame-based approach used by LANET. In the GTE tactical ATM approach, ATM cells are transmitted individually (much like the standard ATM cell-based transmission format) rather than being packed in a frame container (frame-based transmission format). Alternatively, one may consider this as a simplified frame-based format where the frame consists of a single cell. It is in this context that the term "frame" will be used in the remainder of this section.

The standard 424-bit ATM cell is converted into a 503-bit tactical ATM cell, with the header and payload separately encoded with BCH codes. A 5-bit synchronization character is added to the beginning of the tactical ATM cell to produce a 508-bit frame. The detailed structure of the frame is shown in Fig. 21.

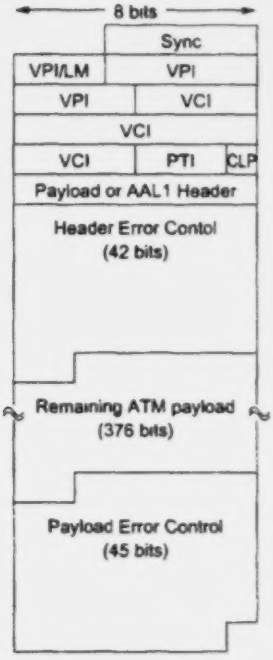


Figure 21: Tactical ATM frame structure.

The header of the tactical ATM cell consists of 40 header bits and 42 header parity-check bits. The header bits include the VPI[3], VCI, PTI and CLP fields (a total of 32 bits), as well as the first eight payload bits of the standard ATM cell. A (82,40) BCH code with 6-bit error-correcting capability is used for error encoding of the header bits. The remaining 376 payload bits are encoded using a (421,376) BCH code with 5-bit error-correcting capability. Thus, 45 payload parity-check bits are included in the tactical ATM cell payload. The choice and performance of the header and payload codes will be discussed in a later subsection.

The reason for protecting the first eight payload bits with the header, separately from the rest of the payload, is that when AAL Type 1 (AAL1) is used for the transport of voice, these

[3]The first three bits of the VPI field may be optionally allocated to Link Management (LM) information.

bits correspond to the AAL1 header. The AAL1 header is important for the processing of the voice payload and is therefore protected with the more powerful header code rather than the payload code.

The overhead due to the frame synchronization character, header, header-error control and payload-error control—excluding the first eight bits of the standard ATM cell which have been incorporated in the header of the tactical ATM cell—accounts for $124/508 = 24.4\%$ of the frame, compared to $40/424 = 9.4\%$ overhead of a standard ATM cell. In the case where payload-error control is not applied, the overhead reduces to $79/463 = 17.1\%$.

The framing character is used for faster cell synchronization/delineation under all channel conditions. Details regarding the framing procedure and its performance are unavailable; it has been stated, however, that frame acquisition/cell delineation processing is typically less than one cell and that the average frame acquisition time is less than three cells for BER $p = 10^{-3}$.

3.2.4 Error-Control Coding

Performance requirements Voice and data applications have different degrees of tolerance to errors and therefore the requirements of each service type are addressed separately.

Continuously Variable Slope Delta (CVSD) modulated voice, commonly used in military applications, is the voice service paradigm considered in the GTE work. CVSD voice at either 16 or 32 kb/s is transmitted with acceptable quality over tactical, non-ATM, LOS links throughout the 10^{-6}–10^{-3} BER range [16]. It is then argued that CVSD voice can be transmitted with acceptable quality over tactical ATM LOS links provided that the error rate *delivered* to the ATM layer remains in the 10^{-6}–10^{-3} range. This implies that voice can tolerate payload errors in this range without significant quality degradation, provided that cells are not lost due to errors in the header, that is, provided that the CLR is maintained low enough. Therefore, the transmission of CVSD voice with acceptable quality over such links can be achieved without the use of payload-error control but requires header-error control to improve the CLR which can take high values as the BER approaches the value 10^{-2} as has been shown in Fig. 4.

Data applications, in general, have more stringent requirements against errors than voice applications. For the efficient bandwidth utilization in the presence of packet retransmissions, it is important that a sufficiently low end-to-end packet-error rate is provided for this type of service. Data packets are segmented into ATM cells for transmission over ATM links and, in order to ensure the desired packet-error rate, both the payload-error rate and the CLR must be maintained sufficiently low. Thus, in the case of data applications, both payload- and header-error control are recommended.

The design provides distinct solutions for voice and data applications. In the case of voice, error control is applied to the header only. The solution proposed for voice, enhanced by payload-error control, is used for data applications. Since the header and payload may have different degrees of tolerance to errors, given the application's QoS requirements, the separate encoding of header and payload provides flexibility and efficiency in the design.

The FEC requirements for the header are determined by the CLR requirements for voice (or other real-time applications), while the FEC requirements for the payload are determined by the end-to-end packet-error rate requirements for data applications.

To maintain high throughput efficiency, close to 100%, for window sizes up to 10 packets, the end-to-end packet-error rate must be no higher than 10^{-2} under all conditions. For packet sizes up to 1060 bytes (or 20 standard ATM cells) and window sizes up to 10 packets, an uncoded throughput efficiency—excluding TCP/IP and ATM overhead—of at least 95% is obtained for channel BERs up to 10^{-6} in the case of the AWGN channel. For larger packet sizes, high throughput efficiency is obtained for lower BERs. For the same packet and window size ranges, an uncoded throughput efficiency above 95% is obtained for channel BERs up to 10^{-5} in the case of the $K = 10$ dB Rician channel. Therefore, the payload code design objective for data transmission is a decoded BER $\leq 10^{-6}$ over the AWGN channel and a decoded BER $\leq 10^{-5}$ over $K = 10$ dB Rician channel.

Error-Control Codes A variety of candidate codes were considered in the GTE study, including punctured convolutional codes, RS codes and BCH codes.

Convolutional Codes The effectiveness of any convolutional code candidate is limited by the requirement for hard-decision decoding. The shortcomings of high-rate, short-constraint-length convolutional codes for tactical ATM applications are briefly discussed in [17]. It is pointed out that a rate-7/8 code obtained by puncturing the rate-1/2, constraint length $K = 7$ code provides a post-decoding BER of 10^{-6} when the channel BER is 1.6×10^{-3}. This performance satisfies the design objective that the delivered BER be less than 10^{-6} for channel BERs up to 10^{-3}, set for tactical ATM applications in [17]. However, short-constraint-length convolutional codes require a significant amount of data interleaving in order to be effective in slow Rician fading and are not considered for tactical ATM as they would violate the latency requirements of voice users.

Reed-Solomon Codes Reed-Solomon codes were also found ineffective for the tactical ATM application. A (64,48) RS code defined on a 6-bit alphabet (6-bit symbols) with error-correcting capability $t = 7$ symbols and code rate $r = 3/4$ will deliver a decoded BER significantly less than the target 10^{-6} for BER 10^{-3} over the AWGN channel. This is, however, achieved at the expense of high overhead. The (64,56) RS code with error-correcting capability $t = 3$ symbols and rate $r = 7/8$ does not meet the target decoded BER. The flexibility in choosing a Reed-Solomon code with optimum trade-off between error-correcting capability and code overhead for given performance requirements is limited by the encoder/decoder sets available by vendors (Reed-Solomon codes with rates $r = 7/8, 3/4$ and $1/2$ are implemented most commonly). Furthermore, a (469,424) binary BCH code with $t = 5$-bit error-correcting capability meets the target decoded BER with code rate $r = 424/469 = 0.9$ which is significantly higher than the rate of (64,48) RS code ($r = 0.75$).

The more fundamental problem with the Reed-Solomon codes is the performance in slow Rician fading. Similarly to the convolutional codes, to make the Reed-Solomon codes effective on this channel would require applying symbol interleaving.

BCH Codes BCH codes provide the best combination of low CLR, low payload-error probability and low overhead for the LOS channel. For relatively short block lengths and moderate error rates, binary BCH codes provide good performance. An important advantage of these

codes is that there exists a wide range of block lengths available for short to moderate length messages and, therefore, the block length can be easily adjusted to match the ATM cell size. The availability of a wide range of block lengths, code rates and error-correcting power for binary BCH codes, as well as the availability of efficient encoding and decoding algorithms, support their use for tactical ATM applications.

Following the testing of binary BCH codes with different error-correcting capabilities,

- a (82,40) code with $t = 6$-bit error-correcting capability was selected for the header, and,
- a (421,376) BCH code with $t = 5$-bit error-correcting capability was selected for the payload.

The performance of the header code with respect to CLR and the performance of the payload code, in terms of the probability P_e that the number of errors in the payload exceeds five, is shown in Table 5 for different channels.

BER	Channel	CLR	P_e
10^{-3}	AWGN	3.6×10^{-12}	5.2×10^{-6}
10^{-3}	Rician ($K = 20$ dB)	1.14×10^{-7}	1.1×10^{-3}
10^{-3}	Rician ($K = 10$ dB)	2.2×10^{-3}	1.7×10^{-3}
10^{-5}	AWGN	3.8×10^{-26}	7.4×10^{-18}
10^{-5}	Rician ($K = 20$ dB)	1.0×10^{-13}	5.5×10^{-9}
10^{-5}	Rician ($K = 10$ dB)	3.2×10^{-5}	1.2×10^{-4}

Table 5: BCH header and payload code performance.

Bit interleaving Interleaving is applied to spread the header bits—with the exception of the synchronization pattern—throughout the cell, and hence, to mitigate the effect of burst errors on the header. It is implemented by placing four payload bits before every header bit, thus creating the following pattern within each frame:

SSSSS-PPPP-H-PPPP-H-PPPP-H-$\cdots$-PPPP-H-PPPPP$\cdots$ PPPP

where S represents a sync bit, P represents a payload bit and H represents a header bit. This results in spreading the header bits throughout $82 \times 4 = 328$ payload bits and having $421 - 328 = 93$ payload bits at the end of the cell following the last header bit. By choosing a spreading distance of four payload bits (instead of five), the same implementation becomes applicable in the case where payload-error control is not employed. In this case, the final header bit is followed by $376 - 328 = 48$ payload bits instead of 93.

4 Recommendations for Error Control Over the Random-Error Channel

The results of the analysis of the FEC-based error-control approaches over the random-error channel presented in Sections 2 and 3.2 are summarized in Table 6 for comparison. In this table, Bandwidth (BW) efficiency η is a measure of the overhead due to header information and error control and is defined as the ratio:

$$\eta = \frac{\text{number of information bits in wireless ATM cell}}{\text{total number of bits in wireless ATM cell}}$$

Code	code rate	η	BER (p)	CLR	$p_{res,b}$
RS (59,53)	0.90	0.81	10^{-3} 10^{-5}	1.3×10^{-3} 1.9×10^{-5}	7.8×10^{-5} 1.1×10^{-12}
BCH (469,424)	0.90	0.82	10^{-3} 10^{-5}	9.6×10^{-6} 1.4×10^{-17}	2.1×10^{-7} 3.3×10^{-19}
BCH (478,424)	0.89	0.80	10^{-3} 10^{-5}	7.2×10^{-7} 1.1×10^{-20}	2.0×10^{-8} 2.9×10^{-22}
BCH (50,32) & BCH (420,384)	0.89	0.82	10^{-3} 10^{-5}	2.2×10^{-7} 2.3×10^{-20}	1.6×10^{-6} 2.3×10^{-16}
BCH (56,32) & BCH (429,384)	0.86	0.79	10^{-3} 10^{-5}	3.7×10^{-9} 3.8×10^{-19}	1.5×10^{-7} 2.1×10^{-19}
DERA (detection)		0.83	10^{-3} 10^{-5}	1.5×10^{-3} 1.6×10^{-7}	
DERA (correction)		0.83	10^{-3} 10^{-5}	3.4×10^{-6} 2.9×10^{-12}	
BCH (82,40) & BCH (421,376)	0.83	0.76	10^{-3} 10^{-5}	3.6×10^{-12} 3.8×10^{-26}	

Table 6: Block code performance over the random-error channel.

Based on the recommendations in [16], the following performance requirements must be satisfied for the transport of voice over tactical ATM LOS links with acceptable quality:

- the CLR must be of the same order of magnitude as the CLR achieved with standard ATM for BERs that are typical of wireline links. For fiber-optic links where, typically, $p \leq 10^{-9}$, CLR $< 10^{-7}$ in pure detection mode. Similarly, for coaxial cable with $p \leq 10^{-7}$, CLR $< 10^{-5}$ (Fig. 4). Therefore, CLR must be less than at least 10^{-5} and, preferably, less than 10^{-7}.

- the error rate delivered to the ATM layer must be less than 10^{-3}.

The above conditions are easily met by the (50,32) BCH header/(420,384) BCH payload code and the (82,40) BCH header/(421,376) BCH payload code schemes. The former combination of header/payload codes with the higher BW efficiency $\eta = 0.79$ is the error-control scheme recommended for the random-error channel.

5 Performance Over the Markov Channel

Section 2 addressed the performance of FEC-based error-control schemes over the random-error channel. The performance of these error-control schemes over the burst-error channel is investigated in this section.

5.1 Introduction

The burst-error channel is modeled using a simple Markov Chain model. Due to their analytical tractability, Markov Chain (MC) models have been used extensively to capture the behavior of the wireless channel and to model the associated *error process*.

5.1.1 Channel Model Description

In the general form, a MC-based model for the channel is associated with an underlying discrete-time Markov chain $\{c_n\}_{n\geq 0}$, where c_n is the state of the channel at time instant n. $\{c_n\}_{n\geq 0}$ is defined on an N-dimensional state space $S = \{0, \ldots, N-1\}$, $N \geq 2$. The time unit associated with the Markov chain is the bit transmission time, although other time units, such as packet transmission time, can be used depending on the channel modeling assumptions and the time scale of interest.

The channel bit-error process $\{e_n\}_{n\geq 1}$ defined by

$$e_n = \begin{cases} 1 & \text{if } n\text{-th bit in error,} \\ 0 & \text{otherwise,} \end{cases} \tag{13}$$

depends, in general, on the state of the channel at time instants $n-1$ and n. That is, the value of the error process at the end of a transition of $\{c_n\}_{n\geq 0}$ from state i to state j ($i \to j$) depends on both states i and j according to the probability distributions

$$p_{1,ij} = \Pr\{e_n = 1, c_n = j | c_{n-1} = i\}, \tag{14}$$

$$p_{0,ij} = \Pr\{e_n = 0, c_n = j | c_{n-1} = i\} = 1 - p_{1,ij}, \tag{15}$$

where $i, j \in S$.

The special case where e_n depends solely on c_n or c_{n-1} is most commonly used in practice because it is easier in this case to associate the parameters of the analytical model to the parameters of the physical channel. The case where e_n depends on c_n only is considered in this work. Then,

$$\begin{aligned} p_{1,ij} &= \Pr\{e_n = 1, c_n = j | c_{n-1} = i\} \\ &= \Pr\{e_n = 1 | c_n = j\} \Pr\{c_n = j | c_{n-1} = i\} \\ &= p_e(j) \Pr\{c_n = j | c_{n-1} = i\}, \end{aligned} \tag{16}$$

where $p_e(j) = \Pr\{e_n = 1 | c_n = j\}$, $0 \leq p_e(j) \leq 1$. That is, given that the state of the channel during the transmission of the n-th bit is j, $c_n = j$, the n-th bit in the bitstream of information is in error with probability $p_e(j)$.

Matrix $\mathbf{P_1}$ with elements $p_{1,ij}$, $i, j \in S$, can be expressed by the matrix product

$$\mathbf{P_1} = \mathbf{P}\mathbf{P_e} \tag{17}$$

where $\mathbf{P}$ is the transition probability matrix of $\{c_n\}_{n\geq 0}$ and $\mathbf{P_e}$ is the diagonal matrix given by $\mathbf{P_e} = diag\{p_e(0), \ldots, p_e(N-1)\}$. Similarly, the matrix with elements $p_{0,ij}$, $i, j \in S$, $\mathbf{P_0}$, can be expressed as

$$\mathbf{P_0} = \mathbf{P}(\mathbf{I} - \mathbf{P_e}), \tag{18}$$

where $\mathbf{I}$ is the identity matrix of dimension N. Note that the finite state Markov Chain channel model is in this case completely defined in terms of the transition probability matrix $\mathbf{P}$ and the error-rate matrix $\mathbf{P_e}$. The channel BER p is given by

$$p = \boldsymbol{\pi}\mathbf{P_e}\mathbf{e}, \tag{19}$$

where $\boldsymbol{\pi}$ is the stationary probability row vector of $\{c_n\}_{n\geq 0}$, $\boldsymbol{\pi} = \boldsymbol{\pi}\mathbf{P}$, $\boldsymbol{\pi}\mathbf{e} = 1$, and $\mathbf{e}$ is the unit column vector of appropriate dimensionality.

5.1.2 Performance Analysis

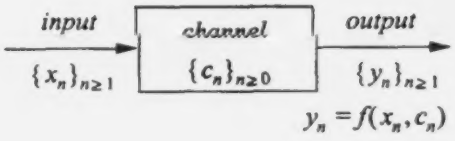
The cell loss and error performance over the Finite State Markov Channel of some of the FEC schemes considered in Section 2 can be analyzed by using Markov Chain theory. Such are the schemes where the ATM cell header is encoded separately from the payload, for reasons that will become obvious from the development of the analysis. Performance bounds can be obtained analytically for schemes such as the NATO PG/6 scheme where header and payload are encoded as a single information block. Simulation results can be obtained in all cases, but for low-error rates these can be computationally intensive and require prohibitively long runtimes.

Fig. 22(a) shows a simple block diagram for the channel where $\{x_n\}_{n\geq 1}$ is the sequence of information bits transmitted over the channel (channel input) and $\{y_n\}_{n\geq 1}$ is the original bit sequence altered by channel errors (channel output). The error process $\{e_n\}_{n\geq 1}$ is illustrated in Fig. 22(b).

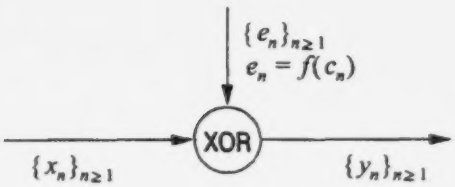
Let u_n denote the number of errors in a block of n bits, $u_n = \sum_{\ell=1}^{n} e_\ell$ and let $\phi_{ij}(k, n)$ be defined as the conditional probability

$$\phi_{ij}(k, n) = \Pr\{c_n = j, u_n = k | c_0 = i\}.$$

That is, $\phi_{ij}(k, n)$ is the probability that the state of the channel during the transmission of the n-th bit is j, $c_n = j$, and that k out of the sequence of n bits $y_1 y_2 \cdots y_n$ are in error, given that the state of the channel before the transmission of the first bit is i, $c_0 = i$. Probabilities $\phi_{ij}(k, n)$



(a) Block diagram



(b) Error process

Figure 22: Channel model.

can be easily obtained for $n \geq 0$, $0 \leq k \leq n$, in a recursive manner:

$$\begin{aligned}
\phi_{ij}(k,n) &= \Pr\{c_n = j, u_n = k | c_0 = i\} \\
&= \sum_{m\in S}\sum_{k'=0}^{1} \Pr\{c_n = j, c_{n-1} = m, u_n = k, e_n = k' | c_0 = i\} \\
&= \sum_{m\in S}\sum_{k'=0}^{1} \Pr\{c_n = j, c_{n-1} = m, u_{n-1} = k-k', e_n = k' | c_0 = i\} \\
&= \sum_{m\in S}\sum_{k'=0}^{1} \Pr\{c_{n-1} = m, u_{n-1} = k-k' | c_0 = i\} \Pr\{e_n = k', c_n = j | c_{n-1} = m\} \\
&= \sum_{m\in S}\sum_{k'=0}^{1} \phi_{im}(k-k', n-1) \Pr\{e_n = k', c_n = j | c_{n-1} = m\} \\
&= \sum_{m\in S} \{\phi_{im}(k, n-1)p_{0,mj} + \phi_{im}(k-1, n-1)p_{1,mj}\}, \qquad (20)
\end{aligned}$$

where $p_{0,mj}$ and $p_{1,mj}$ are given by Eqs. 14 and 15, respectively. Based on Eq. 20, the matrix with elements $\phi_{ij}(k,n)$, $i,j \in S$, denoted by $\mathbf{\Phi}(k,n)$, $n \geq 0$, $0 \leq k \leq n$, can be expressed by the following recursive relationship

$$\mathbf{\Phi}(k,n) = \begin{cases} \mathbf{\Phi}(k,n-1)\mathbf{P_0}, & k = 0, \\ \mathbf{\Phi}(k,n-1)\mathbf{P_0} + \mathbf{\Phi}(k-1,n-1)\mathbf{P_1}, & 0 < k < n, \\ \mathbf{\Phi}(k-1,n-1)\mathbf{P_1}, & k = n, \end{cases} \qquad (21)$$

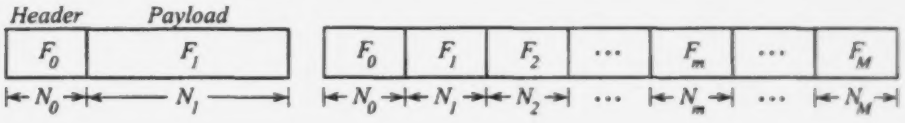
with $\mathbf{\Phi}(0,0) \triangleq \mathbf{I}$.

Probabilities $\mathbf{\Phi}(k,n)$ are useful in deriving performance metrics of interest in different scenarios where forward error correction codes are applied. For example, if information is transmitted over the Markov channel in blocks of size N, then the probability of k errors in the block

is given by $\boldsymbol{\pi}\boldsymbol{\Phi}(k,N)\mathbf{e}$, $0 \le k \le N$. If the information transmitted over the channel is encoded in code blocks of size N, then the probability that the number of errors in the block, U, exceeds the code error-correcting capability t is given by

$$\Pr\{U > t\} = \sum_{k=t+1}^{N} \boldsymbol{\pi}\boldsymbol{\Phi}(k,N)\mathbf{e}.$$

The impact of a channel error on a standard ATM cell and the ATM performance, varies depending on whether the corrupted bit is in the cell header or payload, as has been discussed in Section 1. Recall that the header is protected by a CRC code with single-bit-error-correcting capability while the payload is not protected against errors. Therefore, the analytical study of the performance of ATM over the Markov channel is facilitated by considering the header and payload as two separate fields, F_0 and F_1, respectively, as shown in Fig. 23(a). The size of F_i in bits is denoted by N_i, $i = 0, 1$. For the standard ATM cell, $N_0 = 40$ and $N_1 = 384$.



(a) Standard ATM cell *(b) Generic Wireless ATM cell*

Figure 23: Data block structure for performance analysis.

Let U_i be defined as the number of errors in F_i, $i = 0, 1$:

$$U_i = \sum_{\ell=N_{i-1}+1}^{N_i} e_\ell,$$

where $0 \le U_i \le N_i$ and $N_{-1} \triangleq 0$. Then, the conditional probability

$$\chi_{ij}(k_0,k_1) \triangleq \Pr\{c_{N_0+N_1} = j, U_1 = k_1, U_0 = k_0 | c_0 = i\} \qquad (22)$$
$$i,j \in S, \quad 0 \le k_0 \le N_0, 0 \le k_1 \le N_1,$$

is given by

$$\begin{aligned}\chi_{ij}(k_0,k_1) &= \sum_{m\in S} \Pr\{c_{N_0+N_1} = j, U_1 = k_1 | c_{N_0} = m\} \Pr\{c_{N_0} = m, U_0 = k_0 | c_0 = i\} \\ &= \sum_{m\in S} \phi_{im}(k_0,N_0)\phi_{mj}(k_1,N_1) \\ &= [\boldsymbol{\Phi}(k_0,N_0)\boldsymbol{\Phi}(k_1,N_1)]_{ij}, \end{aligned} \qquad (23)$$

where $[\mathbf{A}]_{ij}$ denotes the (i,j) element of matrix $\mathbf{A}$. Equation 23 can be expressed in matrix form as

$$\mathbf{X}(k_0,k_1) = \boldsymbol{\Phi}(k_0,N_0)\boldsymbol{\Phi}(k_1,N_1), \qquad (24)$$

where $\mathbf{X}(k_0, k_1)$ is the matrix with elements $\chi_{ij}(k_0, k_1)$, $i, j \in S$. Matrices $\mathbf{X}(k_0, k_1)$ are used to obtain the probabilities:

$$\begin{aligned}\Pr\{U_1 = k_1, U_0 = k_0\} &= \sum_{i\in S}\sum_{j\in S} \Pr\{c_{N_0+N_1} = j, U_1 = k_1, U_0 = k_0 | c_0 = i\} \Pr\{c_0 = i\} \\ &= \sum_{i\in S}\sum_{j\in S} \chi_{ij}(k_0, k_1)\pi_i \\ &= \boldsymbol{\pi}\mathbf{X}(k_0, k_1)\mathbf{e} \\ &\triangleq \psi(k_0, k_1)\end{aligned} \tag{25}$$

which, in turn, are used to derive the performance measures of interest.

The results obtained for the standard ATM cell in Eqs. 23 and 25 can be generalized for a data block with the structure shown in Fig. 23(b) which could represent the structure of a generic wireless ATM cell with M fields. The different fields in this generic structure identify cell segments that are encoded using different FEC codes, including no encoding.

In this case, it can be easily shown that,

$$\begin{aligned}\chi_{ij}(k_0, k_1, \ldots, k_M) &\triangleq \Pr\{c_{N_0+N_1+\ldots+N_M} = j, U_M = k_M, \ldots, U_1 = k_1, U_0 = k_0 | c_0 = i\} \\ &\qquad i, j \in S, \quad 0 \le k_m \le N_m, 0 \le m \le M \\ &= [\boldsymbol{\Phi}(k_0, N_0)\boldsymbol{\Phi}(k_1, N_1)\boldsymbol{\Phi}(k_M, N_M)]_{ij},\end{aligned} \tag{26}$$

or equivalently, that

$$\mathbf{X}(k_0, k_1, \ldots, k_M) = \boldsymbol{\Phi}(k_0, N_0)\boldsymbol{\Phi}(k_1, N_1)\ldots\boldsymbol{\Phi}(k_M, N_M). \tag{27}$$

It follows that

$$\begin{aligned}\Pr\{U_1 = k_1, U_0 = k_0, \ldots, U_M = k_M\} &= \boldsymbol{\pi}\mathbf{X}(k_0, k_1, \ldots, k_M)\mathbf{e} \\ &\triangleq \psi(k_0, k_1, \ldots, k_M).\end{aligned} \tag{28}$$

5.1.3 Performance Measures

ATM performance measures of interest can be obtained from the analysis in a straightforward manner. Note that the only type of errors considered in this work are the errors introduced by the wireless channel. The performance measures under consideration are:

- **Cell Loss Ratio (CLR)** defined here as the ratio of lost to total transmitted cells:

$$\text{Cell Loss Ratio} = \frac{\text{lost cells}}{\text{total transmitted cells}}.$$

  Lost cells are cells that are not delivered to the ATM layer by the TC sublayer.

  In the case of standard ATM, lost cells are cells with uncorrectable errors in the header and the CLR is given by:

$$\text{CLR} = \sum_{k_0=t_0+1}^{N_0}\sum_{k_1=0}^{N_1} \psi(k_0, k_1) = 1 - \sum_{k_0=0}^{t_0}\sum_{k_1=0}^{N_1} \psi(k_0, k_1), \tag{29}$$

  where t_0 is the error correcting capability of the header CRC ($t_0 = 1$).

- **Cell Error Ratio (CER)** defined here as the ratio of errored to total transmitted cells:

$$\text{Cell Error Ratio} = \frac{\text{errored cells}}{\text{successfully transmitted cells} + \text{errored cells}}.$$

A received cell is errored if it has an invalid header after header error control procedures have been completed or if the payload is different from the transmitted payload.

For standard ATM cells,

$$\begin{aligned} \text{CER} &= \sum_{k_0=t_0+1}^{N_0} \sum_{k_1=0}^{N_1} \psi(k_0, k_1) + \sum_{k_0=0}^{t_0} \sum_{k_1=1}^{N_1} \psi(k_0, k_1) \\ &= \text{CLR} + \sum_{k_0=0}^{t_0} \sum_{k_1=1}^{N_1} \psi(k_0, k_1) = 1 - \sum_{k_0=0}^{t_0} \psi(k_0, 0). \end{aligned} \tag{30}$$

- **Payload Error Ratio (PER)** defined here as the ratio of errored payload bits to total transmitted payload bits:

$$\text{Payload Error Ratio} = \frac{\text{errored payload bits}}{\text{total transmitted payload bits}}.$$

A received payload bit is errored if it is different from the transmitted payload bit or if it belongs to a cell with an invalid header after header error control procedures. That is, all payload bits of lost cells are considered errored payload bits.

For standard ATM, PER can be expressed as:

$$\text{PER} = \sum_{k_0=t_0+1}^{N_0} \sum_{k_1=0}^{N_1} \psi(k_0, k_1) + \sum_{k_0=0}^{t_0} \sum_{k_1=1}^{N_1} \frac{k_1}{N_1} \psi(k_0, k_1) = \text{CLR} + \sum_{k_0=0}^{t_0} \sum_{k_1=1}^{N_1} \frac{k_1}{N_1} \psi(k_0, k_1). \tag{31}$$

- **Payload Bit Error Ratio (PBER)** defined here as the ratio of errored payload bits delivered to the ATM layer to the total payload bits delivered to the ATM layer:

$$\text{Payload Bit Error Ratio} = \frac{\text{errored payload bits delivered to the ATM layer}}{\text{total payload bits delivered to the ATM layer}}.$$

The PBER is the BER of the payload of the cells that are delivered to the ATM layer.

For standard ATM, the PBER is expressed as:

$$\text{PBER} = \frac{\displaystyle\sum_{k_0=0}^{t_0} \sum_{k_1=1}^{N_1} \frac{k_1}{N_1} \psi(k_0, k_1)}{\displaystyle\sum_{k_0=0}^{t_0} \sum_{k_1=0}^{N_1} \psi(k_0, k_1)}. \tag{32}$$

The performance measures defined above and evaluated in the case of standard ATM can also be evaluated in the case where other FEC schemes are applied for error control as discussed later in this section.

The performance measures of greatest interest in the case of the loss tolerant voice applications are the CLR and the PER.

5.1.4 Performance Over the Gilbert-Elliott Channel

The most simple finite state Markov chain model for the burst-error channel is the *Gilbert-Elliott* (GE) model which is based on a two-state ($N = 2$) Markov chain $\{c_n\}_{n\geq 0}$ with state transition diagram as shown in Fig. 24. The transition probability matrix of $\{c_n\}_{n\geq 0}$ is denoted

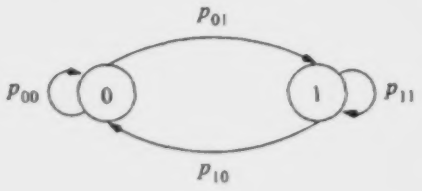


Figure 24: State transition diagram of Gilbert-Elliott channel model.

by

$$\mathbf{P} = \begin{bmatrix} p_{00} & p_{01} \\ p_{10} & p_{11} \end{bmatrix}, \tag{33}$$

and the stationary probability vector is given by

$$\boldsymbol{\pi} = \begin{bmatrix} \pi_0 & \pi_1 \end{bmatrix} = \begin{bmatrix} \dfrac{p_{10}}{p_{01}+p_{10}} & \dfrac{p_{01}}{p_{01}+p_{10}} \end{bmatrix}. \tag{34}$$

The bit-error process $\{e_n\}_{n\geq 1}$ is determined by the underlying Markov chain $\{c_n\}_{n\geq 0}$ as follows: an error in the bit stream occurs with probability $p_e(0)$ whenever $\{c_n\}_{n\geq 0}$ is in state '0' and with probability $p_e(1)$ whenever $\{c_n\}_{n\geq 0}$ is in state '1'. Typically, one state is associated with low bit-error rates (state 0 or *good* state) and the other with high bit-error rates (state 1 or *bad* state), $p_e(0) << p_e(1)$. The channel BER is then given by

$$p = \boldsymbol{\pi}\mathbf{P}_e\mathbf{e} = \pi_0 p_e(0) + \pi_1 p_e(1),\ p_e(0) < p < p_e(1). \tag{35}$$

According to Markov chain theory, the sojourn time in state 1 (0) is geometrically distributed with mean $1/p_{10}$ ($1/p_{01}$) time units. Consequently, the bit-error process $\{e_n\}_{n\geq 1}$ for the GE channel model consists of geometrically distributed '*error-free*' (or low-error rate) periods during which errors are generated randomly with probability $p_e(0)$ followed by geometrically distributed *error-burst* periods with mean $\tau = 1/p_{10}$ during which errors are generated randomly with probability $p_e(1)$. A sample realization of process $\{e_n\}_{n\geq 1}$ is shown in Fig. 25.

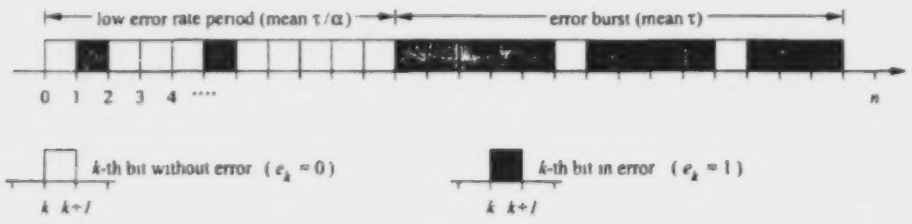


Figure 25: Sample realization of process $\{e_n\}_{n\geq 1}$.

For a given BER p, and selected values for $p_e(0)$ and $p_e(1)$, matrix $\mathbf{P}$ can be expressed in terms of the mean burst length τ as follows:

$$\mathbf{P} = \begin{bmatrix} 1-\alpha/\tau & \alpha/\tau \\ 1/\tau & 1-1/\tau \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} - \frac{1}{\tau}\begin{bmatrix} \alpha & -\alpha \\ -1 & 1 \end{bmatrix}, \tag{36}$$

where $\alpha = \dfrac{p - p_e(0)}{p_e(1) - p}$. The stationary probability vector $\boldsymbol{\pi}$ is independent of τ and given by

$$\boldsymbol{\pi} = \begin{bmatrix} \dfrac{1}{1+\alpha} & \dfrac{\alpha}{1+\alpha} \end{bmatrix} = \begin{bmatrix} \dfrac{p_e(1) - p}{p_e(1) - p_e(0)} & \dfrac{p - p_e(0)}{p_e(1) - p_e(0)} \end{bmatrix}. \tag{37}$$

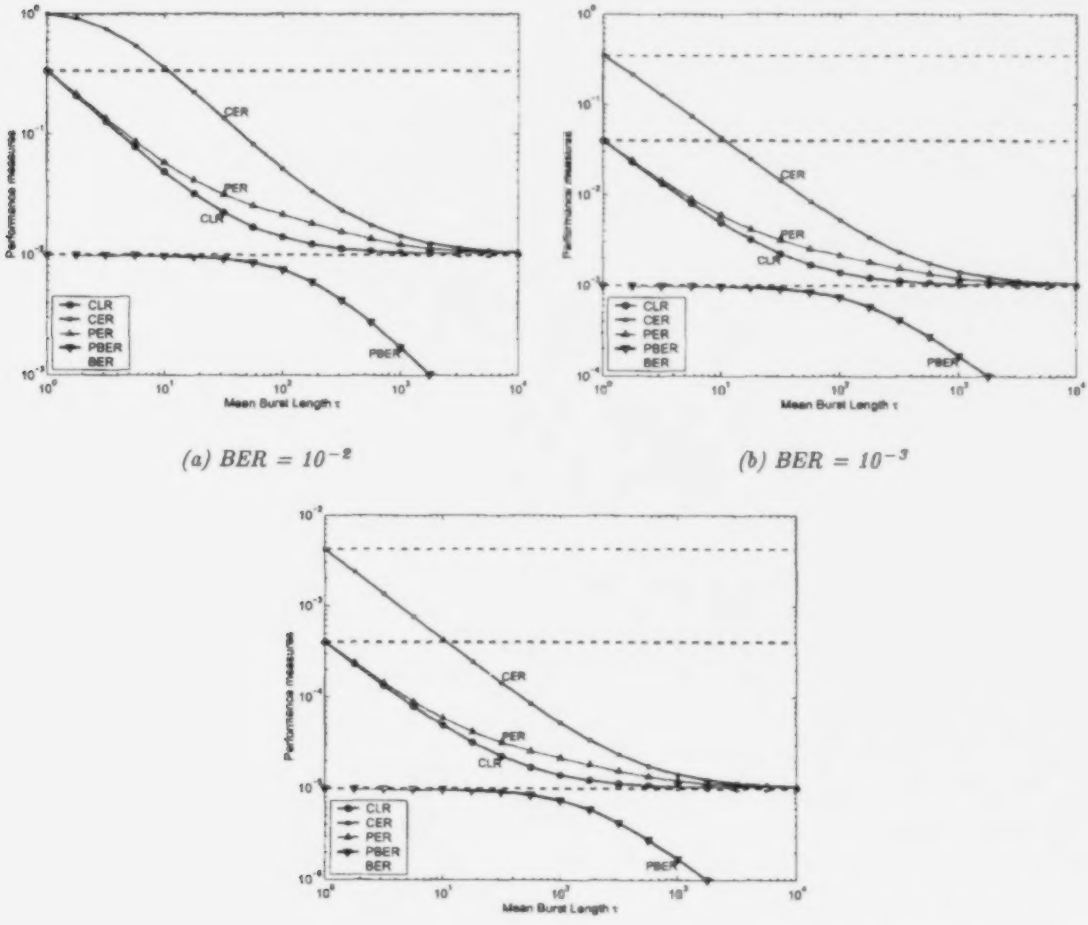
The GE model can be further simplified in terms of the number of parameters involved by considering state 0 to be error-free, i.e., by setting $p_e(0) = 0$.

5.2 Standard ATM

Analytical results for the performance measures discussed in Section 5.1.3 for standard ATM over the GE channel are obtained from Eqs. 29 - 32. The channel is characterized by an error-rate matrix $\mathbf{P}_e = diag\{0, 1\}$ and transition probability matrix $\mathbf{P}$ given by Eq. 36.

5.2.1 Error-Detection Mode

The performance of standard ATM with Header Error Check (HEC) in detection mode (no header-error correction) is shown in Fig. 26 for different values of BER p. For all measures of



(a) BER = 10^{-2}

(b) BER = 10^{-3}

(c) BER = 10^{-5}

Figure 26: Analytical results for standard ATM over the GE channel in HEC detection mode.

interest, the performance over the GE channel is improved compared to that over the random-error channel (dashed lines).

More specifically, for standard ATM in detection mode, the CLR is given by

$$\mathrm{CLR} = 1 - \boldsymbol{\pi}\mathbf{P}_0{}^{N_0}\mathbf{e}. \tag{38}$$

Equation 38 is obtained by applying the following relationships to Eqs. 24 and 25:

$$\sum_{k_1=0}^{N_1} \boldsymbol{\Phi}(k_1, N_1) = \mathbf{P}^{N_1}, \quad \boldsymbol{\Phi}(0, N_0) = \mathbf{P}_0{}^{N_0}. \tag{39}$$

As $\tau \to 1$, CLR approaches its value obtained over the random-error channel. From Eq. 36,

$$\mathbf{P} \to \begin{bmatrix} 1-\alpha & \alpha \\ 1 & 0 \end{bmatrix}, \quad \text{as } \tau \to 1. \tag{40}$$

Consequently, $\mathrm{CLR} \to \mathrm{CLR}_1 = 1 - \pi_0(1-\alpha)^{N_0-1} = 1 - (1-p)(1-\alpha)^{N_0-1}$. When $p \ll 1$, $\alpha \approx p$ and $\mathrm{CLR}_1 \approx 1-(1-p)^{N_0}$, the CLR value over the random-error channel. It can be easily shown that as $\tau \to \infty$, $\mathbf{P} \to \mathbf{I}$ and $\mathrm{CLR} \to \mathrm{CLR}_\infty = \pi_1 = p$. That is, for the GE channel with $\mathbf{P}_e = diag\{0, 1\}$, CLR approaches the link BER as the mean burst length τ increases.

The improvement of CLR performance with respect to the random-error channel can intuitively be explained as follows. In the random-error channel, all cells have the same probability of being discarded due to errors. This is not the case for the GE channel, where errors are grouped in bursts. The error-free time interval between error-bursts in the GE channel is longer than the time interval between errors in the random-error channel, for the same link BER. These longer intervals result in fewer cells being discarded in the GE channel than in the random-error channel for the same BER.

Following arguments similar to those used above to establish the CLR behavior for limiting values of τ, it can be shown that for $p \ll 1$:

$$\lim_{\tau\to 1} \mathrm{CER} = 1 - (1-p)(1-\alpha)^{N_0+N_1-1} \approx 1 - (1-p)^{N_0+N_1},$$
$$\lim_{\tau\to 1} \mathrm{PER} \approx \mathrm{CLR} + p(1-\mathrm{CLR}) \approx \mathrm{CLR},$$
$$\lim_{\tau\to 1} \mathrm{PBER} \approx p.$$

It can also be shown that

$$\lim_{\tau\to\infty} \mathrm{CER} = \mathrm{CLR} = p, \quad \lim_{\tau\to\infty} \mathrm{PER} = \mathrm{CLR} = p, \quad \lim_{\tau\to\infty} \mathrm{PBER} = 0. \tag{41}$$

For large values of τ the main contribution to CER comes from the CLR; that is, for large error-bursts, cells with no errors in the header are most likely to have no errors in the payload. However, the key contributing factor to CER for small values of τ, are cells with error-free header and errored payload.

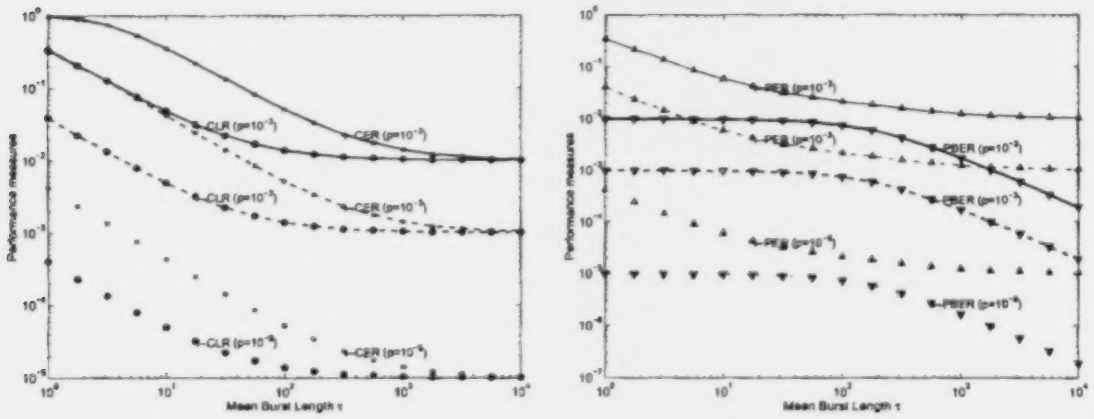
PER takes values that are slightly higher than CLR, implying that CLR is the dominant factor of PER. This highlights the significance of payload bits lost due errors in the header and the need to avoid cell discarding.

For small values of τ, the payload BER of undiscarded cells (PBER) is equal to the link BER p. As the burst length increases, undiscarded cells tend to have error-free payload and the PBER decreases to zero.

Note that, for each performance measure, the results obtained for two values of p that differ by some order of magnitude are also different by approximately that same order of magnitude. That is,

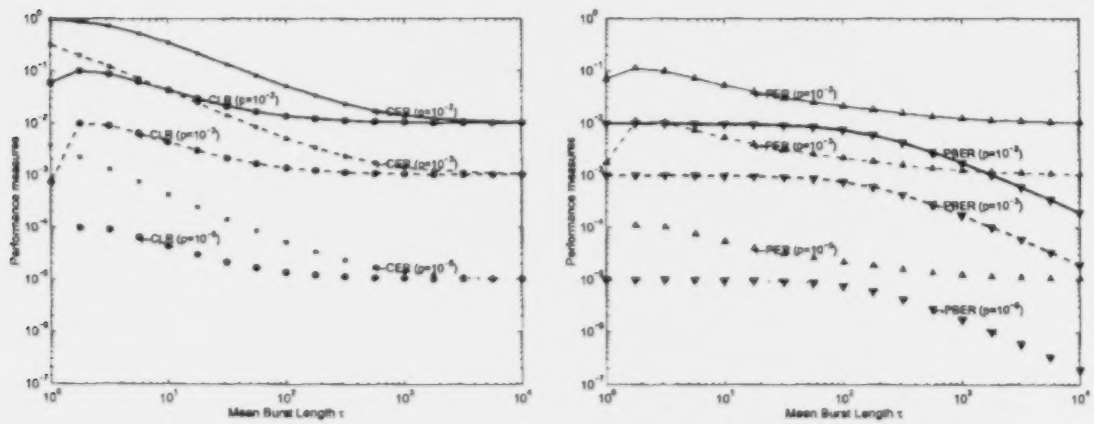
$$\frac{\mathrm{CLR}(p_1)}{\mathrm{CLR}(p_2)} \approx \frac{p_1}{p_2}$$

where $\mathrm{CLR}(p_i)$ denotes the CLR value evaluated at $p = p_i$, $i = 1, 2$. In other words, the results for a given performance measure for different values of p are represented by parallel lines on a logarithmic scale, as illustrated in Fig. 27.



(a) Results for CLR and CER *(b) Results for PER and PBER*

Figure 27: Analytical results for standard ATM over the GE channel in HEC detection mode.



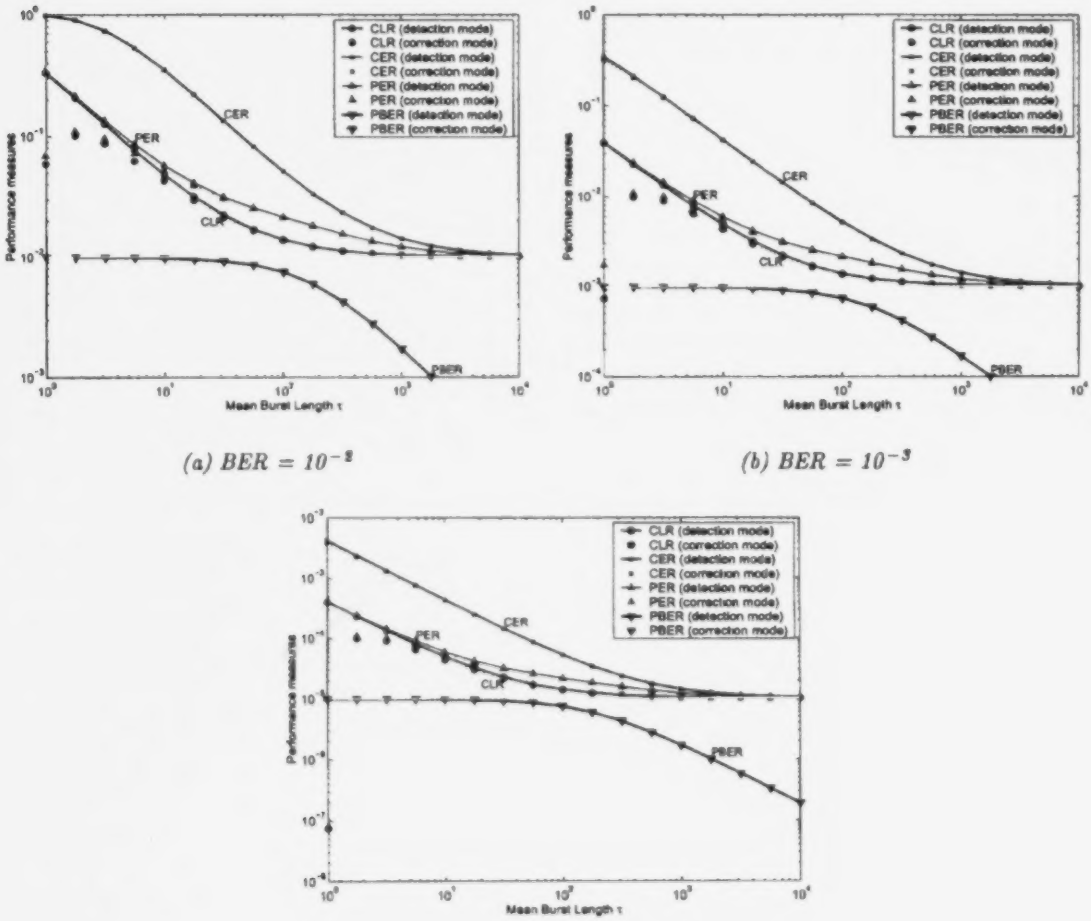
(a) Results for CLR and CER *(b) Results for PER and PBER*

Figure 28: Analytical results for standard ATM over the GE channel in HEC correction mode.

5.2.2 Error-Correction Mode

A performance behavior similar to the one exhibited in detection mode (Fig. 27) is observed when HEC is in correction mode for $\tau \geq 2$ (Fig. 28).

The performance of standard ATM with respect to CLR and PER for small values of τ improves when HEC is used in correction mode (dotted lines in Fig. 29), most noticeably for $\tau = 1$. For large error-bursts, the single-bit error-correcting capability of the header is ineffective.



(a) BER = 10^{-2}

(b) BER = 10^{-3}

(c) BER = 10^{-5}

Figure 29: Analytical results for standard ATM over the GE channel in HEC detection and correction modes.

Note that CLR is the dominant factor of PER as discussed in the case of HEC detection mode (Section 5.2.1), as long as the CLR value remains above BER p. When CLR $\ll p$, the PER value is dominated by p, as is the case for $p = 10^{-5}$, $\tau = 1$ in correction mode (Fig. 29(c)).

The CER and PBER measures remain largely unaffected by the error-correcting capability of the header. In the case of CER, this is due to the fact that CLR is not the dominant factor of CER for small values of τ. In the case of PBER, header-error correction results in fewer cells being discarded, but does not affect the payload BER of the cells.

5.3 NATO PG/6 Proposal

5.3.1 Performance of Cell RS Codes

Analytical results for the performance metrics of interest (CLR,CER,PER and PBER) cannot be obtained in the case of the NATO PG/6 proposal, which uses a (59,53) RS code to protect the entire ATM cell. An upperbound for the CER, and consequently for the CLR, is found in the probability that the number of errored symbols per codeword (coded ATM cell) exceeds the code error-correcting capability t:

$$\text{CLR} \leq \text{CER} \leq \text{CLR}_u = \Pr\{\text{number of errored codeword symbols} > t\},$$

where

$$\text{CLR}_u = \sum_{k=t+1}^{N} \boldsymbol{\pi}\mathbf{V}(k,N)\mathbf{e}, \quad N = 59, \tag{42}$$

$$\mathbf{V}(k,n) = \begin{cases} \mathbf{V}(k,n-1)\mathbf{V}_0, & k = 0, \\ \mathbf{V}(k,n-1)\mathbf{V}_0 + \mathbf{V}(k-1,n-1)\mathbf{V}_1, & 0 < k < n, \\ \mathbf{V}(k-1,n-1)\mathbf{V}_1, & k = n, \end{cases} \tag{43}$$

with $\mathbf{V}_0 = \boldsymbol{\Phi}(0,m)$, $\mathbf{V}_1 = \sum_{k=1}^{m} \boldsymbol{\Phi}(k,m)$ $(m = 8)$ and $\mathbf{V}(0,0) \triangleq \mathbf{I}$.

In addition, the residual BER is a lowerbound for the PER:

$$\text{BER}_{res} \leq \text{PER},$$

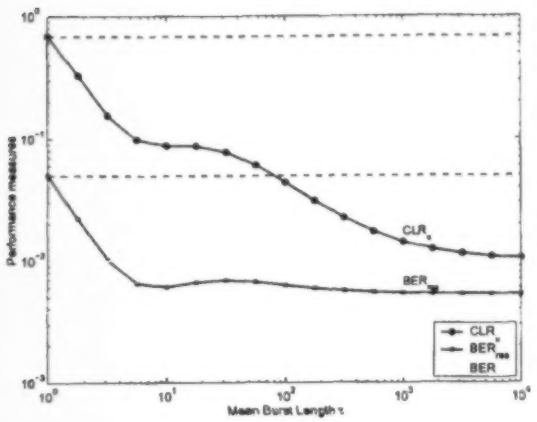
where

$$\text{BER}_{res} = \frac{2^{m-1}}{2^m - 1} \sum_{k=t+1}^{N} \frac{k+t}{N} \boldsymbol{\pi}\mathbf{V}(k,N)\mathbf{e}. \tag{44}$$

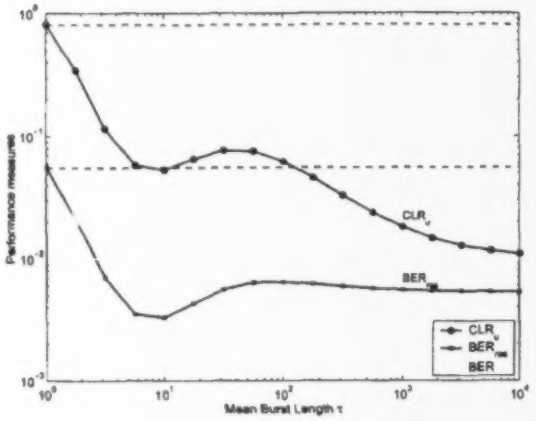
Analytical results for CLR_u and BER_{res} for the (59,53) RS code as obtained from Eqs. 42 and 44 are shown in Figs. 30(a), 30(c) and 30(e) for different values of p, $p = 10^{-2}, 10^{-3}, 10^{-5}$. The corresponding results for the (118,106) RS code are shown in Figs. 30(b), 30(d) and 30(f). The dashed lines in Fig. 30 correspond to the results for the random-error channel.

From the analytical results presented in Fig. 30 it is observed that for $\tau \lessapprox 20$ and $p \leq 10^{-3}$ the (118,106) RS code gives significantly improved results compared to the (59,53) RS code, especially as $\tau \to 1$.

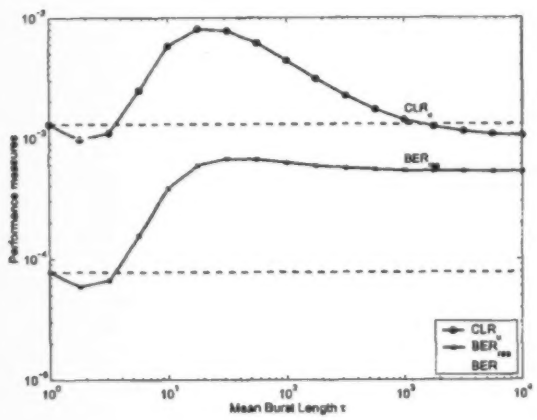
Simulation results for CLR, CER, PER and PBER for the (59,53) RS code at $p = 10^{-3}$ are shown in Fig. 31(b) for HEC operation in detection mode (dm - solid curves) and in mixed mode (mm - dashed curves). Note that for large values of τ there is little improvement in using mixed mode instead of detection mode.



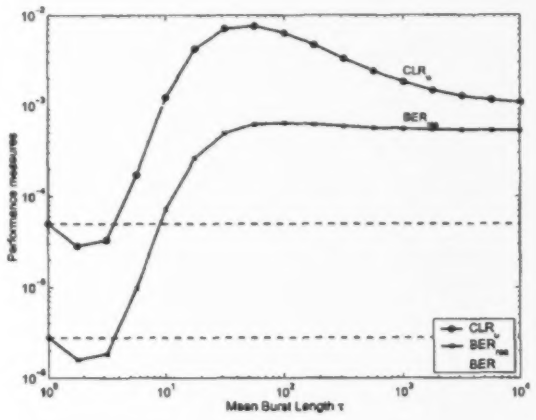
(a) (59,53) RS - BER = 10^{-2}



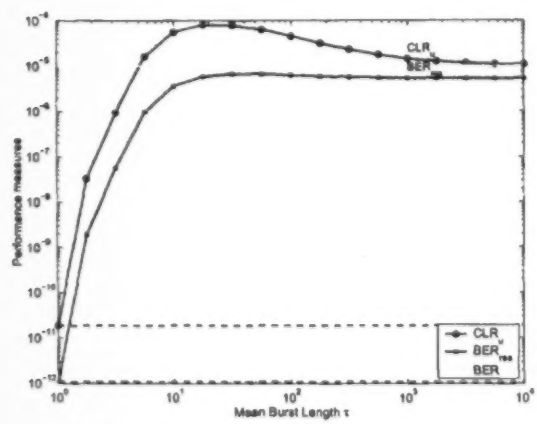
(b) (118,106) RS - BER = 10^{-2}



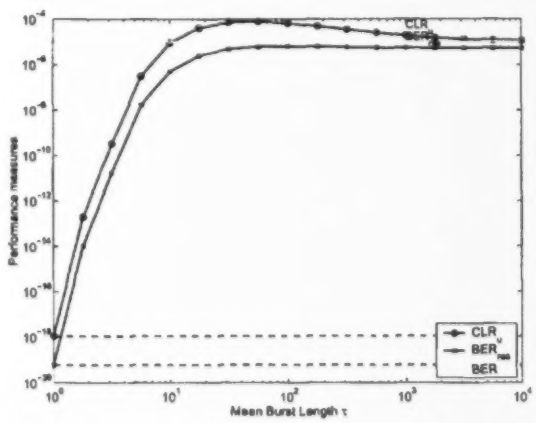
(c) (59,53) RS - BER = 10^{-3}



(d) (118,106) RS - BER = 10^{-3}

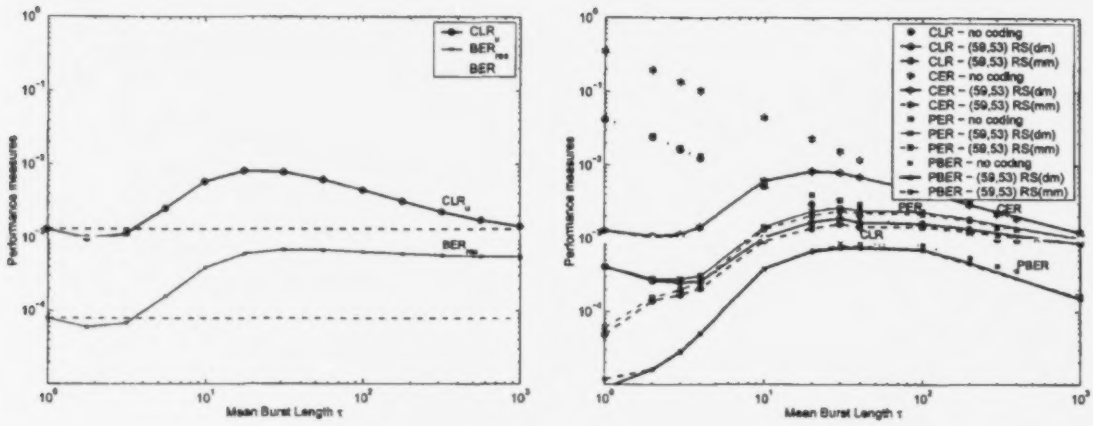


(e) (59,53) RS - BER = 10^{-5}



(f) (118,106) RS - BER = 10^{-5}

Figure 30: Analytical results for the PG/6 error-control scheme over the GE channel.



(a) Analytical results - BER = 10^{-3} *(b) Simulation results - BER = 10^{-3}*

Figure 31: Analytical and simulation results for the (59,53) RS code over the GE channel.

The results for the analytical bounds are presented for comparison purposes in Fig. 31(a). Note that CLR_u is a tight bound for CER but quite loose for CLR. Furthermore, the simulation results for CLR, CER and PER in detection mode take values that lie between the curves for the analytical bounds.

The dotted lines in Fig. 31(b) represent the results for standard ATM in detection mode. The effect of the RS code on the performance decreases with the increase of τ and is most significant for $\tau < 20$. For values of τ sufficiently large, the use of coding becomes ineffective, with performance deteriorating to levels below those achieved when no coding is used. For example, in the case of CLR shown in Fig. 31(b), this takes place for $\tau < 200$. The fact that, for large error-bursts, there are fewer cells discarded when no error coding is used can be explained as follows. In the case of the RS code, a wireless ATM cell corrupted by a sufficiently long error-burst will always be discarded regardless of the location of the errored bits in the cell. This is due to the error-correcting capability of the code being exceeded. In the case where no coding is used, the same error burst will result in a discarded cell only when the burst corrupts the standard ATM cell header.

The performance of a code with given error-correcting capability over a channel with fixed BER depends on the way errors are "distributed" among the wireless ATM cells (codewords). For a given BER, performance is best over the channel where the distribution of errors is such that the code error-correcting capability is reached but not exceeded for the largest possible number of cells. If the BER is high enough that the error-correcting capability has to be exceeded, then, performance is best if errors are clustered within a cell so that a discarded cell carries as many corrupted bits as possible.

In the case of the (59,53) RS code, for small values of p, such as $p = 10^{-5}$, performance is better over the random-error channel than over the GE channel for the entire range of τ (Fig. 30(e)). For large values of p, such as $p = 10^{-2}$, performance over the GE channel is better than over the random-error channel for the entire range of τ (Fig. 30(a)). For $p = 10^{-3}$, performance is better over the GE channel for small values of τ and better over the random-error channel for large values of τ (Fig. 30(c)).

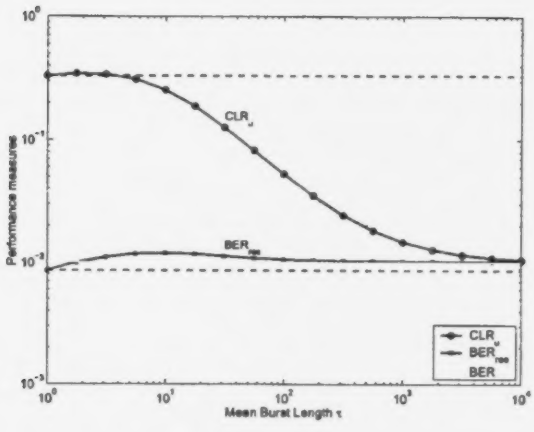
5.3.2 Performance of Cell BCH Codes

The performance of BCH codes when applied to the entire ATM cell is considered in this subsection. The message block subject to encoding is the standard ATM cell of length 424 bits. In the case of an (N, K) BCH code with error-correcting capability t, CLR_u and BER_{res} are given by Eqs. 45 and 46, respectively:

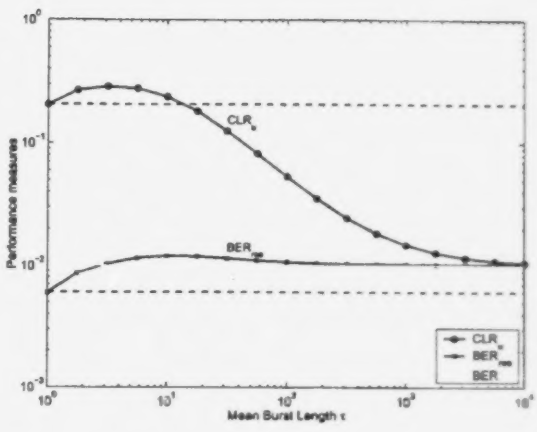
$$\mathrm{CLR}_u = \sum_{k=t+1}^{N} \pi\Phi(k, N)\mathbf{e}, \tag{45}$$

$$\mathrm{BER}_{res} = \sum_{k=t+1}^{N} \frac{k+t}{N}\pi\Phi(k, N)\mathbf{e}. \tag{46}$$

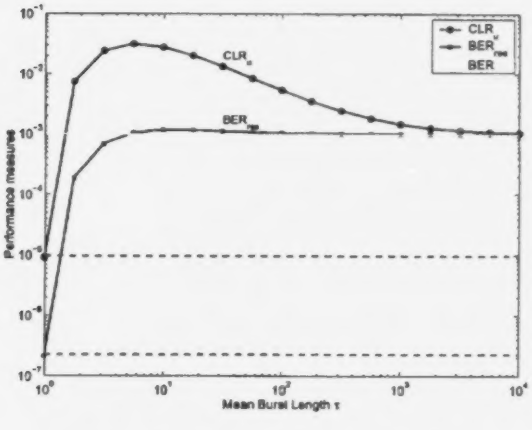
Analytical results for CLR_u and BER_{res} for the (469,424) BCH code ($t = 5$) are shown in Figs. 32(a), 32(c) and 32(e) for different values of p, $p = 10^{-2}$, 10^{-3}, 10^{-5}. The corresponding results for the (478,424) BCH code ($t = 6$) are shown in Figs. 32(b), 32(d) and 32(f). The dashed lines in Fig. 32 correspond to the results for the random-error channel.



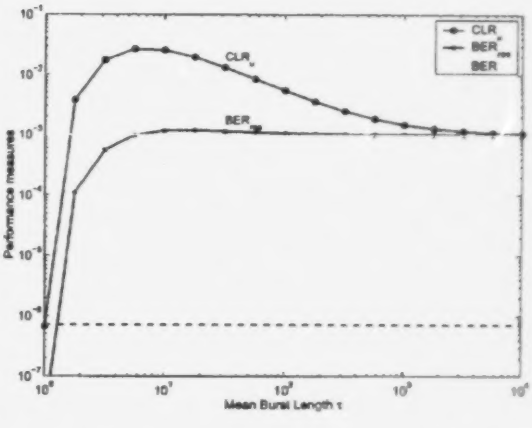
(a) (469,424) BCH - BER = 10^{-2}



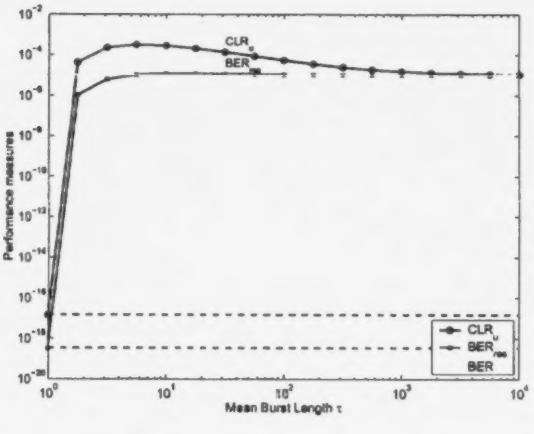
(b) (478,424) BCH - BER = 10^{-2}



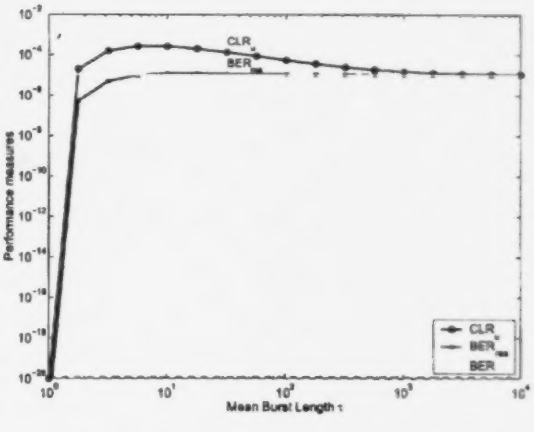
(c) (469,424) BCH - BER = 10^{-3}



(d) (478,424) BCH - BER = 10^{-3}



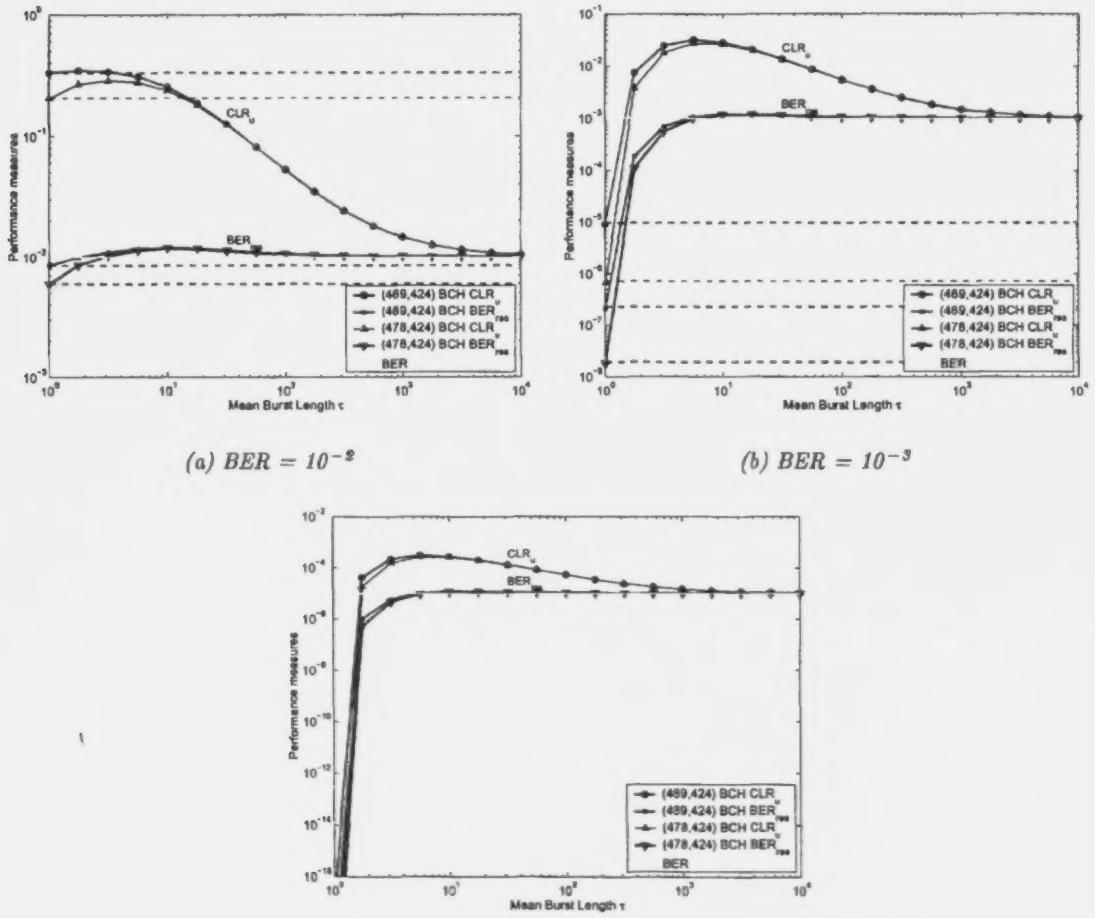
(e) (469,424) BCH - BER = 10^{-5}



(f) (478,424) BCH - BER = 10^{-5}

Figure 32: Analytical results for the (469,424) BCH and (478,424) BCH codes over the GE channel.

The performance of these two codes which is compared directly in Fig. 33, identifies the shortcomings of BCH codes in the burst-error environment: the performance improvement achieved by increasing the error correcting capability of the code by one bit is insignificant over the entire range of τ with the exception of $\tau = 1$. For $\tau = 1$, the (478,424) BCH code outperforms the (469,424) BCH code and the performance improvement increases with the decrease of the BER, a behavior well-anticipated in view of the performance of BCH codes over the random-error channel.



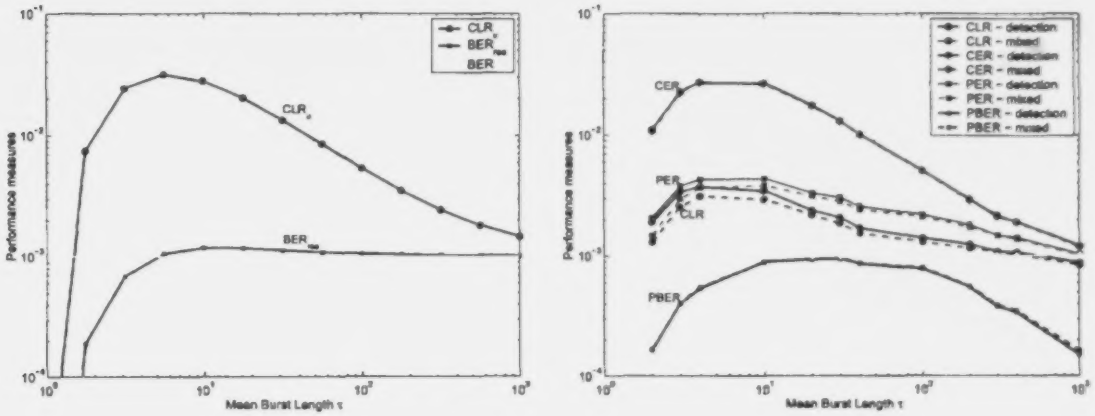
(a) BER = 10^{-2}

(b) BER = 10^{-3}

(c) BER = 10^{-5}

Figure 33: Comparison of analytical results for the (469,424) BCH and (478,424) BCH codes over the GE channel.

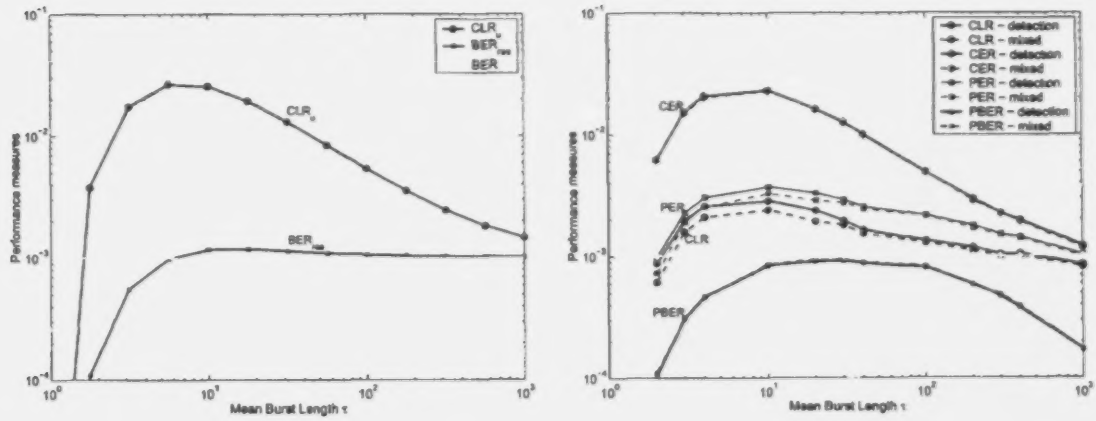
Simulation results for the CLR, CER, PER and PBER for the (469,424) BCH code are shown in Fig. 34(b) next to the analytical results for the CLR_u and BER_{res} shown in Fig. 34(a). The results shown in Fig. 34 are for $p = 10^{-3}$. The solid curves in Fig. 34(b) represent the results for detection mode HEC operation while the dashed curves the results for mixed mode. Note that, similarly to the case of RS codes, there is little improvement in using mixed mode for values of τ greater than one.



(a) Analytical results - BER = 10^{-3} *(b) Simulation results - BER = 10^{-3}*

Figure 34: Analytical and simulation results for the (469,424) BCH code over the GE channel.

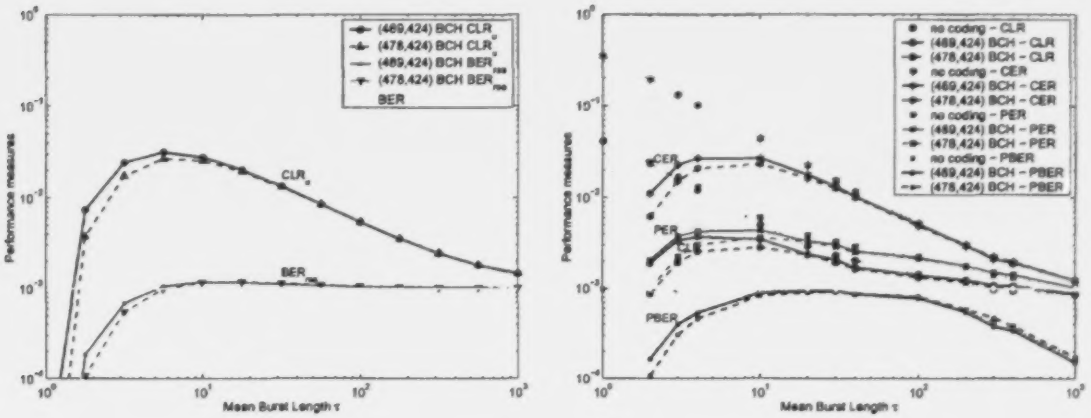
Similar observations can be made in the case of the (478,424) BCH code. Analytical and simulation results for the (478,424) BCH code for $p = 10^{-3}$ are shown in Figs. 35(a) and 35(b), respectively.



(a) Analytical results - BER = 10^{-3} *(b) Simulation results - BER = 10^{-3}*

Figure 35: Analytical and simulation results for the (478,424) BCH code over the GE channel.

Simulation results for the (469,424) BCH code in detection mode are shown in Fig. 36(b) (solid lines). The corresponding results for the (478,424) BCH code are shown in the same figure in dashed lines. The comparison of these results confirms the performance behavior observed based on the analytical bounds: for $\tau > 1$, the increase of the code error-correcting capability yields small improvement in the performance measures under consideration.



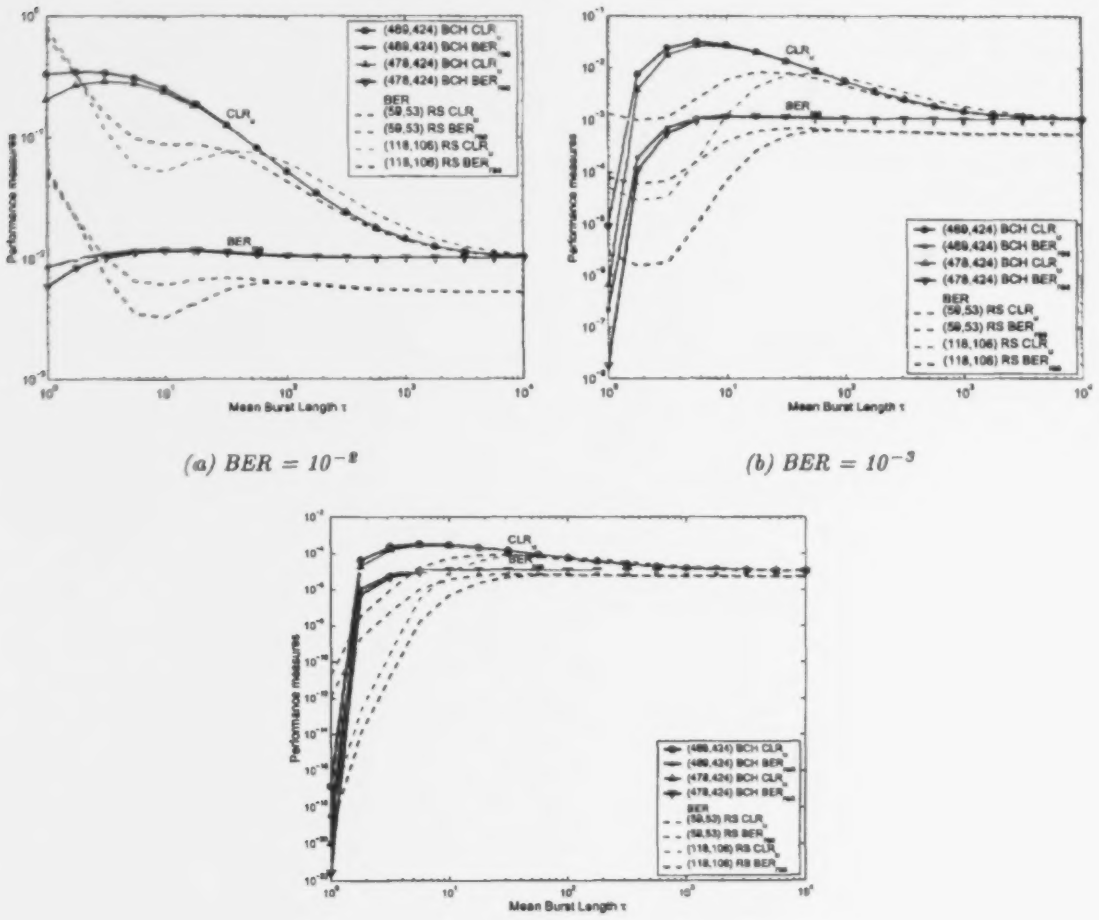
(a) Analytical results - BER = 10^{-3} *(b) Simulation results - BER = 10^{-3}*

Figure 36: Analytical and simulation results for the (469,424) BCH and (478,424) BCH codes over the GE channel.

For τ roughly greater than 200, the BCH codes, much like the RS codes considered in the previous section, become ineffective, resulting in performance that is worse than that when no encoding is used. The effect of the codes is most significant for τ less than approximately 20 and increases with decreasing values of τ. For $\tau < 20$, all performance measures decrease monotonically for decreasing values of τ. It is worthwhile mentioning that this is not always the case with RS codes where some of the measures may decrease and then increase with decreasing τ, as shown in Fig. 31(b). This difference in performance behavior is attributed to the nonbinary nature of Reed-Solomon codes and is exhibited for τ less than the code symbol length m ($m = 8$).

5.3.3 Performance Comparison of RS and BCH Codes

The analytical results for the RS and BCH codes considered in Sections 5.3.1 and 5.3.2, respectively, are compared in Fig. 37. For convenience, the performance comparison results for the RS and BCH codes with respect to the CLR_u and the BER_{res} bounds are also tabulated in Table 7.



(a) BER = 10^{-2}

(b) BER = 10^{-3}

(c) BER = 10^{-5}

Figure 37: Comparison of analytical results for the RS and BCH codes over the GE channel.

In this table, the relation $x \underset{m}{\prec} y$, where x, y are codes and m is a performance metric, $m \in \{\mathrm{CLR}_u, \mathrm{BER}_{res}\}$, is used to indicate that code x is outperformed by code y with respect to metric m:

$$x \underset{m}{\prec} y \equiv \{\text{code } x \text{ outperformed by code } y \text{ with respect to metric } m\}.$$

For example, (118,106) RS $\underset{\mathrm{CLR}_u}{\prec}$ (59,53) RS indicates that (118,106) RS is outperformed by (59,53)

RS with respect to CLR_u, i.e., the value of CLR_u for (118,106) RS is higher than that for (59,53) RS.

The key code performance observations with respect to CLR_u and BER_{res} from Fig. 37 are captured in Table 7 and summarized as follows:

- The performance with respect to CLR_u and BER_{res} does not differ significantly for τ greater than approximately 30 ($\tau \gtrapprox 30$), with the most significant differences between RS and BCH codes appearing in the range of τ for less than approximately 30 ($\tau \lessapprox 30$).
- For $\tau = 1$ and $p = 10^{-2}$, BCH codes and RS codes, in particular, perform extremely poorly. For $\tau = 1$, the best choice of code for both CLR_u and BER_{res} is the (478,424) BCH code.
- For $2 \lessapprox \tau \lessapprox 30$, RS codes outperform BCH codes and the best choice for both CLR_u and BER_{res} is the (118,106) RS code.

BER	τ	CLR_u
10^{-2}	$\tau = 1$	(118,106) RS $\underset{\mathrm{CLR}_u}{\prec}$ (59,53) RS $\underset{\mathrm{CLR}_u}{\prec}$ (469,424) BCH $\underset{\mathrm{CLR}_u}{\prec}$ (478,424) BCH
10^{-2}	$2 \lessapprox \tau \lessapprox 30$	(469,424) BCH $\underset{\mathrm{CLR}_u}{\prec}$ (478,424) BCH $\underset{\mathrm{CLR}_u}{\prec}$ (59,53) RS $\underset{\mathrm{CLR}_u}{\prec}$ (118,106) RS
10^{-2}	$100 \lessapprox \tau$	(118,106) RS $\underset{\mathrm{CLR}_u}{\prec}$ (478,424) BCH $\underset{\mathrm{CLR}_u}{\prec}$ (469,424) BCH $\underset{\mathrm{CLR}_u}{\prec}$ (59,53) RS
10^{-3}	$\tau = 1$	(59,53) RS $\underset{\mathrm{CLR}_u}{\prec}$ (118,106) RS $\underset{\mathrm{CLR}_u}{\prec}$ (469,424) BCH $\underset{\mathrm{CLR}_u}{\prec}$ (478,424) BCH
10^{-3}	$2 \lessapprox \tau \lessapprox 30$	(469,424) BCH $\underset{\mathrm{CLR}_u}{\prec}$ (478,424) BCH $\underset{\mathrm{CLR}_u}{\prec}$ (59,53) RS $\underset{\mathrm{CLR}_u}{\prec}$ (118,106) RS
10^{-3}	$100 \lessapprox \tau$	(118,106) RS $\underset{\mathrm{CLR}_u}{\prec}$ (478,424) BCH $\underset{\mathrm{CLR}_u}{\prec}$ (469,424) BCH $\underset{\mathrm{CLR}_u}{\prec}$ (59,53) RS
10^{-5}	$\tau = 1$	(59,53) RS $\underset{\mathrm{CLR}_u}{\prec}$ (469,424) BCH $\underset{\mathrm{CLR}_u}{\prec}$ (118,106) RS $\underset{\mathrm{CLR}_u}{\prec}$ (478,424) BCH
10^{-5}	$2 \lessapprox \tau \lessapprox 30$	(469,424) BCH $\underset{\mathrm{CLR}_u}{\prec}$ (478,424) BCH $\underset{\mathrm{CLR}_u}{\prec}$ (59,53) RS $\underset{\mathrm{CLR}_u}{\prec}$ (118,106) RS
10^{-5}	$100 \lessapprox \tau$	(118,106) RS $\underset{\mathrm{CLR}_u}{\prec}$ (478,424) BCH $\underset{\mathrm{CLR}_u}{\prec}$ (469,424) BCH $\underset{\mathrm{CLR}_u}{\prec}$ (59,53) RS
BER	τ	BER_{res}
10^{-2}	$\tau = 1$	same as for CLR_u
10^{-2}	$2 \lessapprox \tau \lessapprox 30$	same as for CLR_u
10^{-2}	$100 \lessapprox \tau$	(478,424) BCH $\underset{\mathrm{BER}_{res}}{\prec}$ (469,424) BCH $\underset{\mathrm{BER}_{res}}{\prec}$ (118,106) RS $\underset{\mathrm{BER}_{res}}{\prec}$ (59,53) RS
10^{-3}	$\tau = 1$	same as for CLR_u
10^{-3}	$2 \lessapprox \tau \lessapprox 30$	same as for CLR_u
10^{-3}	$100 \lessapprox \tau$	(478,424) BCH $\underset{\mathrm{BER}_{res}}{\prec}$ (469,424) BCH $\underset{\mathrm{BER}_{res}}{\prec}$ (118,106) RS $\underset{\mathrm{BER}_{res}}{\prec}$ (59,53) RS
10^{-5}	$\tau = 1$	same as for CLR_u
10^{-5}	$2 \lessapprox \tau \lessapprox 30$	same as for CLR_u
10^{-5}	$100 \lessapprox \tau$	(478,424) BCH $\underset{\mathrm{BER}_{res}}{\prec}$ (469,424) BCH $\underset{\mathrm{BER}_{res}}{\prec}$ (118,106) RS $\underset{\mathrm{BER}_{res}}{\prec}$ (59,53) RS

Table 7: Comparison of analytical results for the RS and BCH codes over the GE channel.

The comparison of the simulation results for the (59,53) RS and the (469,424) BCH codes for $p = 10^{-3}$ and HEC operation in detection mode is shown in Fig. 38. These results are shown for $\tau \geq 2$ as it is computationally prohibitive to obtain simulation results for the low probabilities occurring at $\tau = 1$. Summarizing the performance observations for the (59,53) RS

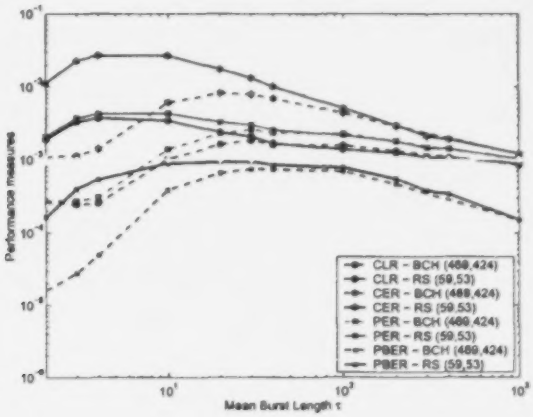


Figure 38: Comparison of simulation results for the RS and BCH codes over the GE channel.

code and the (469,424) BCH code over the GE channel from the simulation results, the RS code performs better over the entire range of τ where the use of coding is effective except for $\tau = 1$. The RS and BCH codes have approximately the same bandwidth efficiency η:

$$\eta_{RS} = \frac{384}{59 \times 8} = 0.814, \quad \eta_{BCH} = \frac{384}{469} = 0.819.$$

5.4 Combination Header/Payload FEC

Analytical results for the CLR, CER, PER and PBER for error-control schemes where FEC is applied independently to the header and payload can be easily obtained based on the analysis presented in Section 5.1.2. If an (N_0,K_0) BCH code with error-correcting capability t_0 is used for the header and an (N_1,K_1) BCH code with error-correcting capability t_1 is used for the payload, the performance measures of interest are obtained from the following expressions:

$$\text{CLR} = \sum_{k_0=t_0+1}^{N_0}\sum_{k_1=0}^{N_1}\psi(k_0,k_1) = 1 - \sum_{k_0=0}^{t_0}\sum_{k_1=0}^{N_1}\psi(k_0,k_1) \tag{47a}$$

$$\begin{aligned}\text{CER} &= \sum_{k_0=t_0+1}^{N_0}\sum_{k_1=0}^{N_1}\psi(k_0,k_1) + \sum_{k_0=0}^{t_0}\sum_{k_1=t_1+1}^{N_1}\psi(k_0,k_1) \\ &= \text{CLR} + \sum_{k_0=0}^{t_0}\sum_{k_1=t_1+1}^{N_1}\psi(k_0,k_1) = 1 - \sum_{k_0=0}^{t_0}\sum_{k_1=0}^{t_1}\psi(k_0,k_1)\end{aligned} \tag{47b}$$

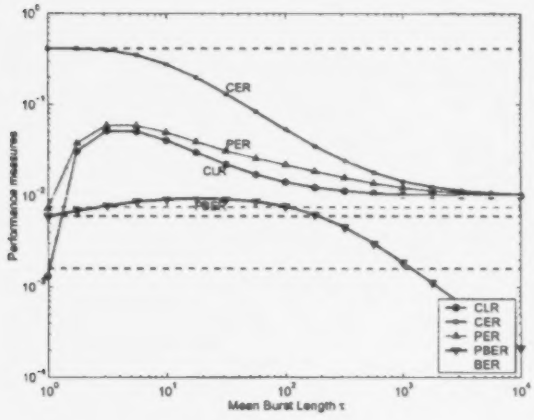
$$\begin{aligned}\text{PER} &= \sum_{k_0=t_0+1}^{N_0}\sum_{k_1=0}^{N_1}\psi(k_0,k_1) + \sum_{k_0=0}^{t_0}\sum_{k_1=t_1+1}^{N_1}\frac{k_1}{N_1}\psi(k_0,k_1) \\ &= \text{CLR} + \sum_{k_0=0}^{t_0}\sum_{k_1=t_1+1}^{N_1}\frac{k_1}{N_1}\psi(k_0,k_1)\end{aligned} \tag{47c}$$

$$\text{PBER} = \frac{\displaystyle\sum_{k_0=0}^{t_0}\sum_{k_1=t_1+1}^{N_1}\frac{k_1}{N_1}\psi(k_0,k_1)}{\displaystyle\sum_{k_0=0}^{t_0}\sum_{k_1=0}^{N_1}\psi(k_0,k_1)}, \tag{47d}$$

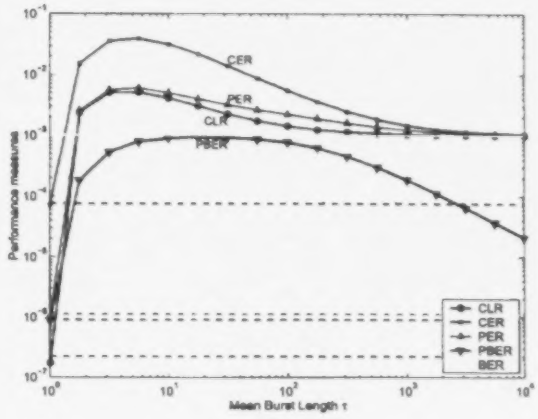
where $\psi(k_0,k_1) = \boldsymbol{\pi}\boldsymbol{\Phi}(k_0,N_0)\boldsymbol{\Phi}(k_1,N_1)\mathbf{e}$.

5.4.1 Performance of (50,32) BCH Header/(420,384) BCH Payload Codes

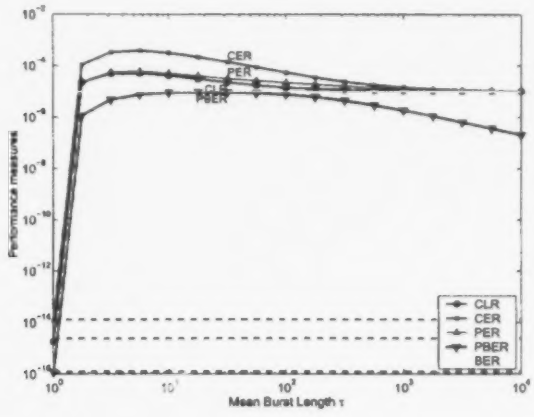
Analytical results for the combination of (50,32) BCH header code ($t_0 = 3$) and (420,384) BCH payload code ($t_1 = 4$) for different values of p, $p = 10^{-2}, 10^{-3}, 10^{-5}$ are shown in Fig. 39.



(a) BER = 10^{-2}



(b) BER = 10^{-3}

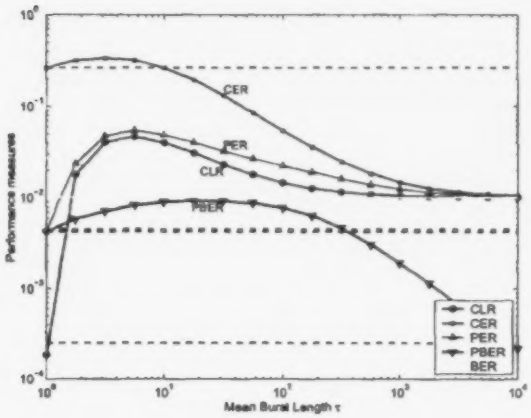


(c) BER = 10^{-5}

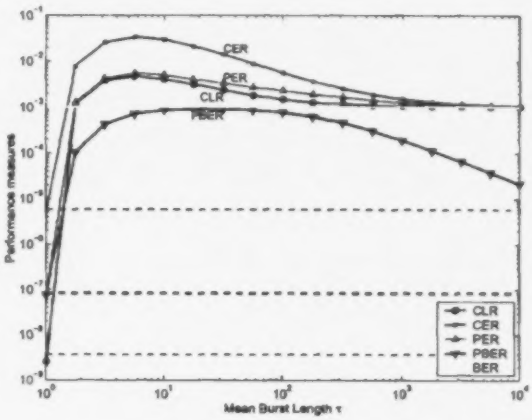
Figure 39: Analytical results for the (50,32) BCH header/(420,384) BCH payload codes over the GE channel.

5.4.2 Performance of (56,32) BCH Header/(429,384) BCH Payload Codes

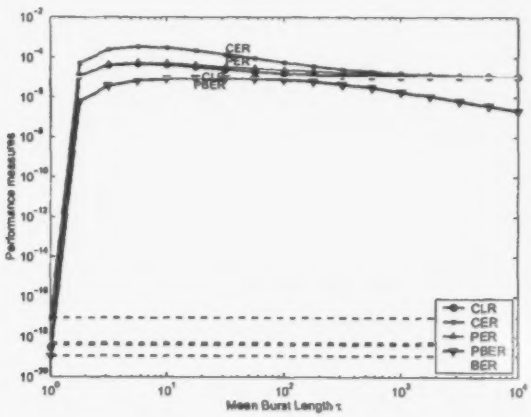
Fig. 40 shows analytical results for the combination of (56,32) BCH header code ($t_0 = 4$) and (429,384) BCH payload code ($t_1 = 5$) for BER $p = 10^{-2}, 10^{-3}, 10^{-5}$.



(a) BER = 10^{-2}



(b) BER = 10^{-3}

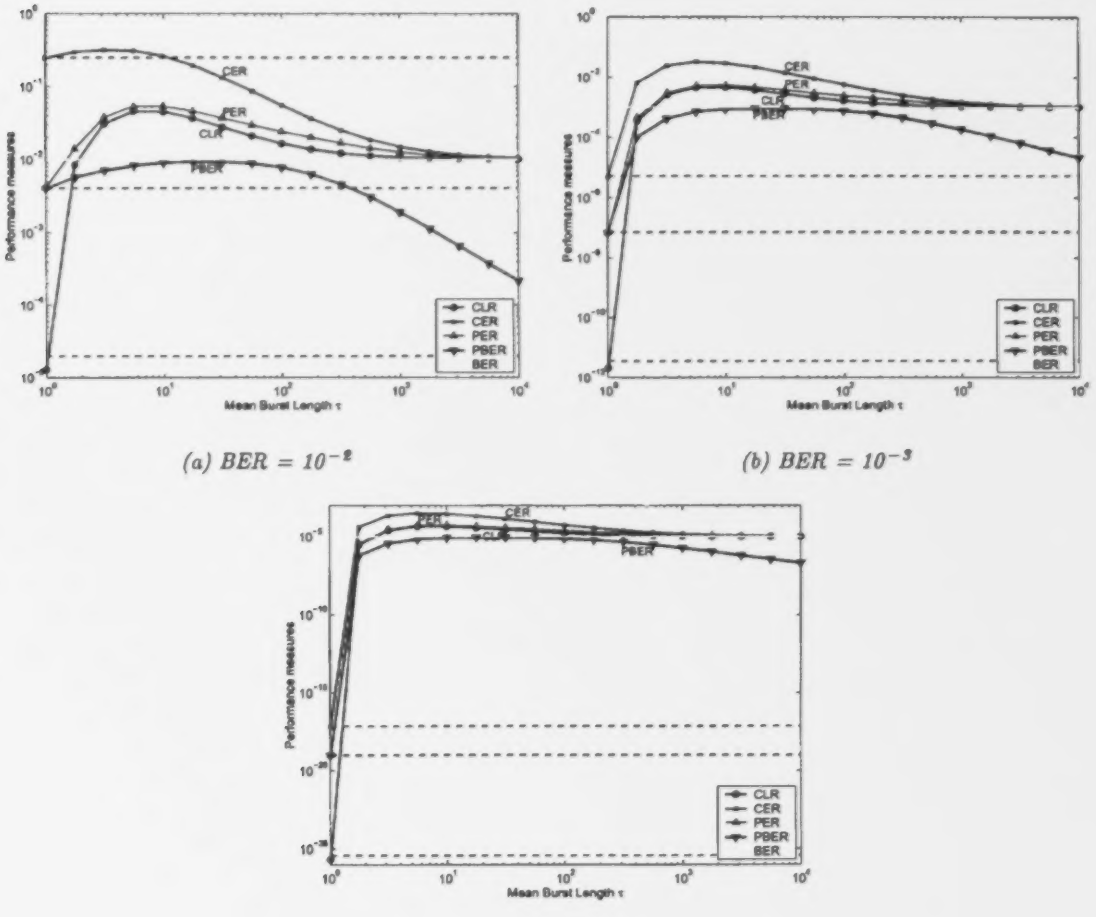


(c) BER = 10^{-5}

Figure 40: Analytical results for the (56,32) BCH header/(429,384) BCH payload codes over the GE channel.

5.4.3 Performance of (82,40) BCH Header/(421,376) BCH Payload Codes

Analytical results for the FEC scheme adopted for tactical ATM in the GTE proposal are shown in Fig. 41 for different values of BER p.



(a) BER = 10^{-2}

(b) BER = 10^{-3}

(c) BER = 10^{-5}

Figure 41: Analytical results for the (82,40) BCH header/(421,376) BCH payload codes over the GE channel.

5.4.4 Performance of (56,32) BCH Header/(224,192) BCH Payload Codes

In the NTT proposal the ATM cell payload is divided into two blocks of equal size $K_1 = K_2 = 192$ which are individually encoded using identical BCH codes. Let N_1, N_2 be the codeword length of the two BCH codes and let t_1, t_2 be the respective code error-correcting capability. Assuming that the header is encoded separately using an (N_0, K_0) BCH code, the performance measures of interest are obtained as follows:

$$\text{CLR} = \sum_{k_0=t_0+1}^{N_0} \sum_{k_1=0}^{N_1} \sum_{k_2=0}^{N_2} \psi(k_0, k_1, k_2) \tag{48a}$$

$$\text{CER} = \text{CLR} + \sum_{k_0=0}^{t_0} \sum_{k_1=0}^{t_1} \sum_{k_2=t_2+1}^{N_2} \psi(k_0, k_1, k_2) + \sum_{k_0=0}^{t_0} \sum_{k_1=t_1+1}^{N_1} \sum_{k_2=0}^{N_2} \psi(k_0, k_1, k_2) \tag{48b}$$

$$\text{PER} = \text{CLR} + \text{PER}_2 \tag{48c}$$

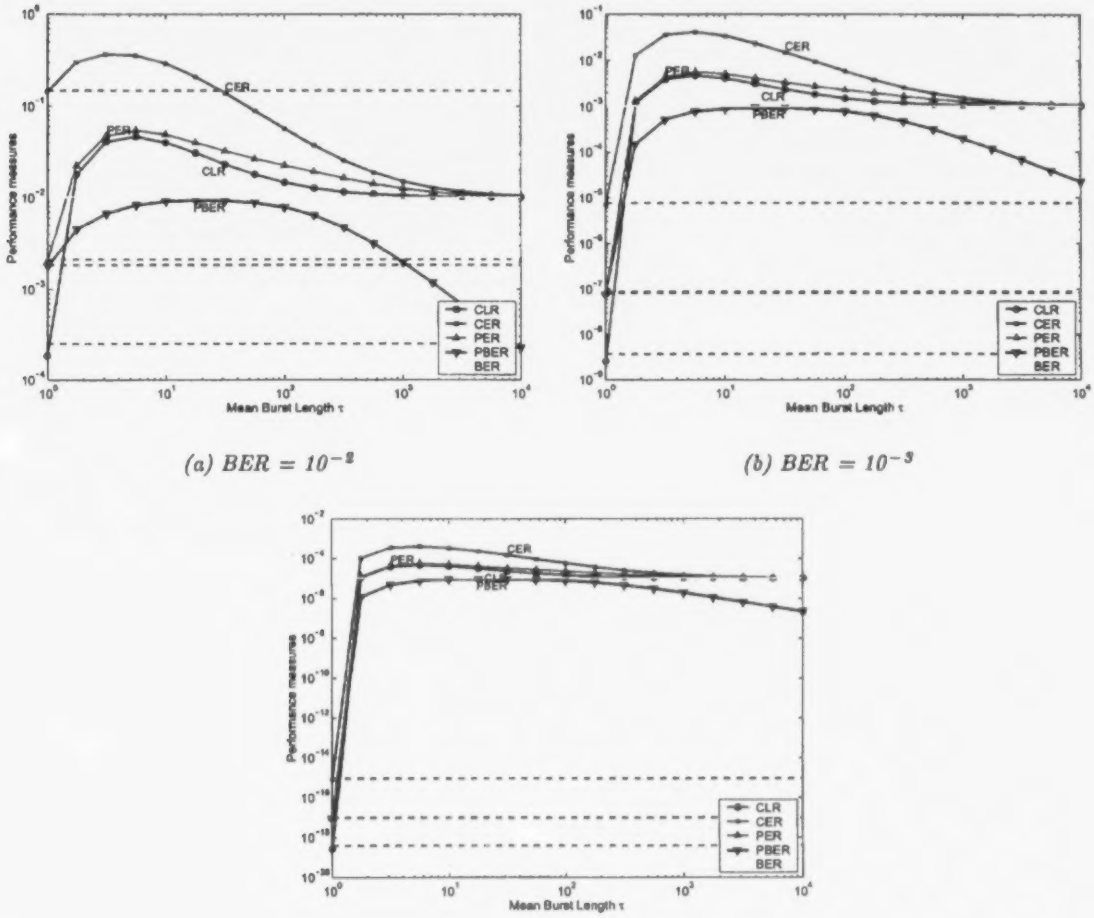
$$\text{PBER} = \frac{\text{PER}_2}{\sum_{k_0=0}^{t_0} \sum_{k_1=0}^{N_1} \sum_{k_2=0}^{N_2} \psi(k_0, k_1, k_2)}, \tag{48d}$$

where PER_2 is the payload-error rate of the undiscarded ATM cells and is given by

$$\text{PER}_2 = \sum_{k_0=0}^{t_0} \Bigg\{ \sum_{k_1=0}^{t_1} \sum_{k_2=t_2+1}^{N_2} \frac{k_2}{N_1+N_2} \psi(k_0, k_1, k_2) + \sum_{k_1=t_1+1}^{N_1} \sum_{k_2=0}^{t_2} \frac{k_1}{N_1+N_2} \psi(k_0, k_1, k_2) + \sum_{k_1=t_1+1}^{N_1} \sum_{k_2=t_2+1}^{N_2} \frac{k_1+k_2}{N_1+N_2} \psi(k_0, k_1, k_2) \Bigg\},$$

and $\psi(k_0, k_1, k_2) = \pi \Phi(k_0, N_0) \Phi(k_1, N_1) \Phi(k_2, N_2) \mathbf{e}$.

Analytical results for the combination of (56,32) BCH header code ($N_0 = 56$, $t_0 = 4$) and the (224,192) BCH payload code ($N_1 = N_2 = 224$, $t_1 = t_2 = 4$) for BER $p = 10^{-2}, 10^{-3}, 10^{-5}$ are shown in Fig. 42.



(a) BER = 10^{-2}

(b) BER = 10^{-3}

(c) BER = 10^{-5}

Figure 42: Analytical results for the combination (56,32) BCH header code and (224,192) BCH payload code over the GE channel.

5.4.5 Performance Comparison of Combination Header/Payload FEC

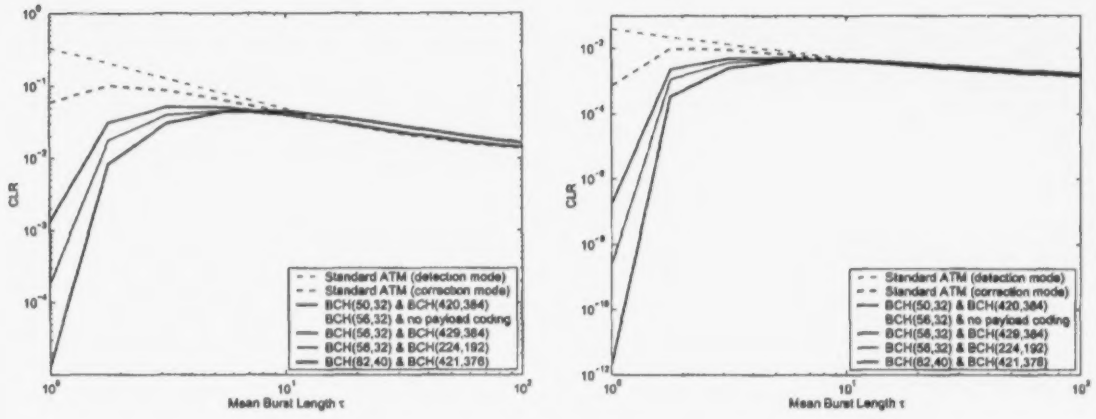
The performance behavior of the error-control schemes considered in this section with respect to CLR, CER, PER and PBER is summarized in Figs. 43-46.

One key characteristic of this behavior is that, for values of τ larger than approximately 10 bits, all schemes have performance with respect to all measures that is almost identical to the performance of standard ATM. More specifically, for large values of τ, standard ATM in correction mode outperforms the other schemes with respect to all performance measures except for PBER. The best PBER performance for large values of τ is achieved by standard ATM in detection mode.

For τ less than approximately 10:

- The GTE scheme ((82,40) BCH header/(421,376) BCH payload codes) exhibits the best CLR performance (Fig. 43).

  The second best CLR performance is exhibited by the schemes that use the (56,32) BCH header code[4].



(a) BER = 10^{-2} *(b) BER = 10^{-3}*

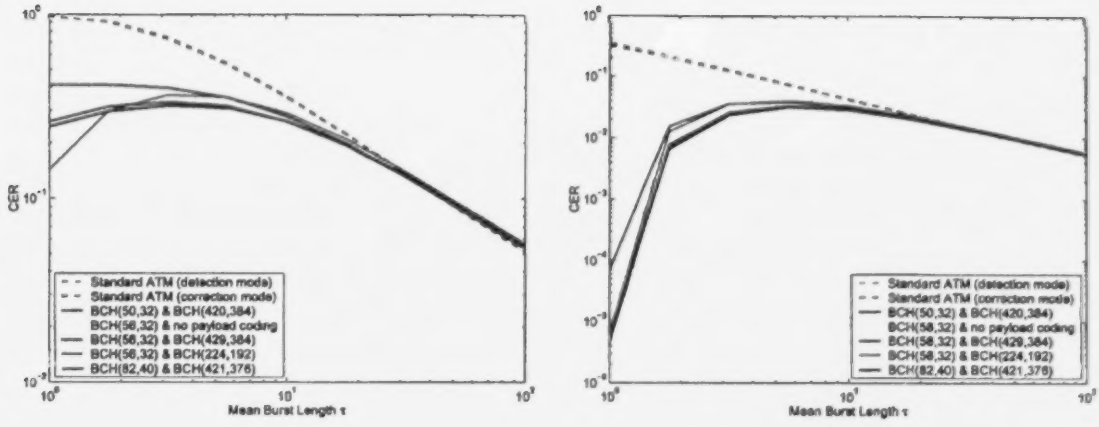
Figure 43: Performance comparison of CLR for combination header/payload BCH codes.

- The GTE scheme exhibits the best CER performance except for values of τ close to one and $p > 10^{-3}$, where it is outperformed by the NTT scheme which encodes the payload in two separate data blocks (Fig. 44).

  This performance is very closely matched by that of the (56,32) BCH header/(429,384) BCH payload code scheme.

- Similar to the CER performance, the best PER performance is exhibited by the GTE scheme except for large values of p ($p > 10^{-3}$) and small values of τ ($\tau \approx 1$) (Fig. 45).

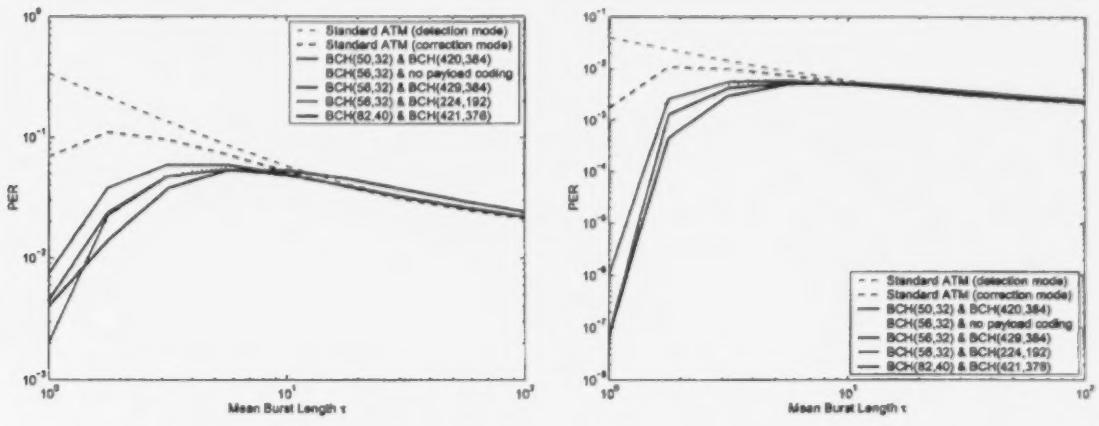
[4]Note that schemes with the same header code ((56,32) BCH) have the same CLR performance.



(a) BER = 10^{-2} *(b) BER = 10^{-3}*

Figure 44: Performance comparison of CER for combination header/payload BCH codes.

The PER performance of the (56,32) BCH/(429,384) BCH scheme is comparable to that of the NTT scheme except for values of τ close to one. In this case, the former scheme performs better for small values of p, while the latter performs better for large values of p.

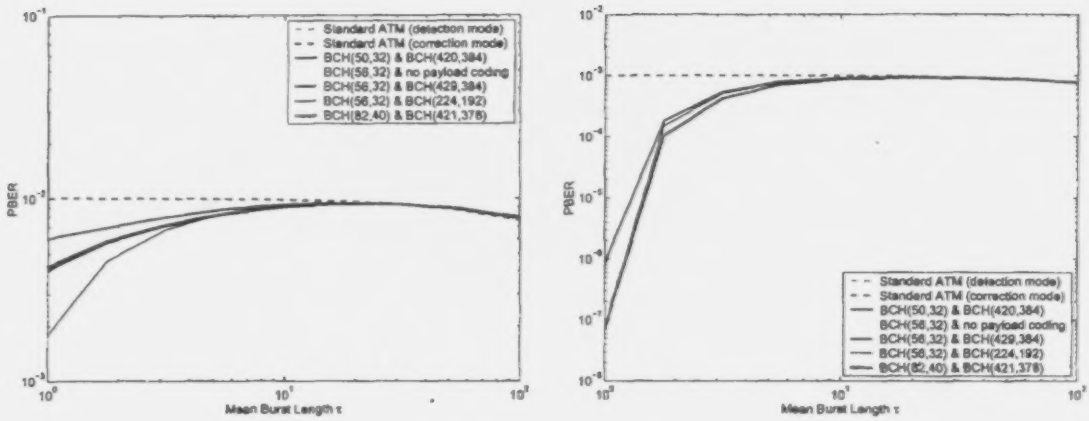


(a) BER = 10^{-2} *(b) BER = 10^{-3}*

Figure 45: Performance comparison of PER for combination header/payload BCH codes.

- The GTE scheme exhibits the best PBER performance (Fig. 46) except for large values of p where it is outperformed by the NTT scheme.

  The PBER performance of the (56,32) BCH/(429,384) BCH scheme is very close to that of the GTE scheme.



(a) BER = 10^{-2} *(b) BER = 10^{-3}*

Figure 46: Performance comparison of PBER for combination header/payload BCH codes.

- Note that the CER performance of the (56,32) BCH header code with no payload coding is identical to that of standard ATM. The same for the PBER performance.

  The PER performance improves if payload coding is combined with the (56,32) BCH code of the header. The improvement is most significant for small values of p ($p \leq 10^{-3}$) and τ ($\tau \approx 1$). For $\tau \geq 2$ payload coding does not improve the PER performance significantly.

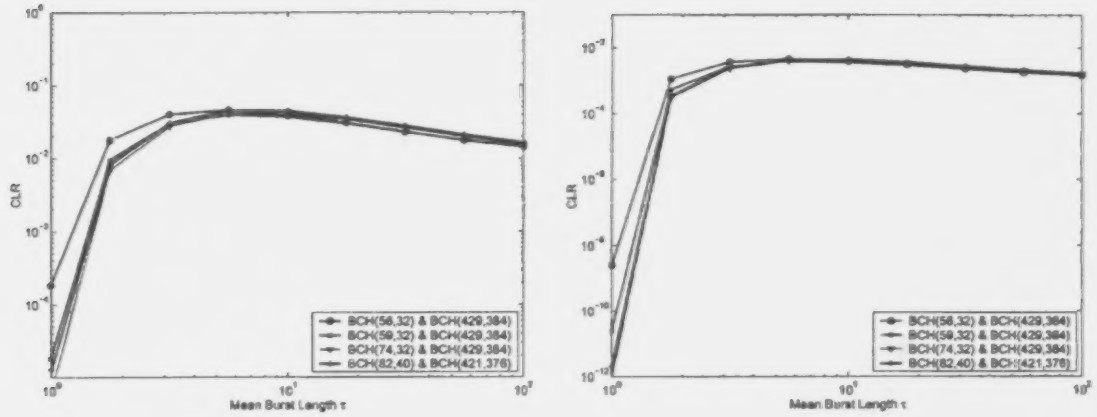
In summary, for $p \leq 10^{-3}$, the GTE scheme with BW efficiency $\eta = 384/503 = 0.763$ has the best overall performance, followed by the combination (56,32) BCH header/(429,384) BCH payload code scheme with efficiency $\eta = 384/485 = 0.792$.

Recall that the GTE scheme uses a header code with error-correcting capability $t_0 = 6$ and a payload code with error-correcting capability $t_1 = 5$. The (56,32) BCH header/(429,384) BCH payload code scheme has $t_0 = 4$ and $t_1 = 5$. The strength of the header code is increased to $t_0 = 5$ for the (59,32) BCH code and to $t_0 = 6$ for the (74,32) BCH code. These codes combined with the (429,384) BCH code for the payload result in schemes with BW efficiency $\eta = 384/488 = 0.789$ and $\eta = 384/503 = 0.763$, respectively.

The relative performance of these schemes as the strength of the header code increases while the strength of the payload code is maintained the same is shown in Figs. 47- 50 for different values of p. The figure also show the performance of the GTE scheme for comparison purposes. It is worthwhile noting that, for values of τ close to one, the CLR, CER and PER performance improves with t_0. The opposite is true for the PBER performance. These fine details are indistinguishable in the figures as the performance of all schemes is comparable for all measures except for the CLR and small values of τ. Furthermore, the effect of the header code on the CER and PBER performance is insignificant for all practical purposes.

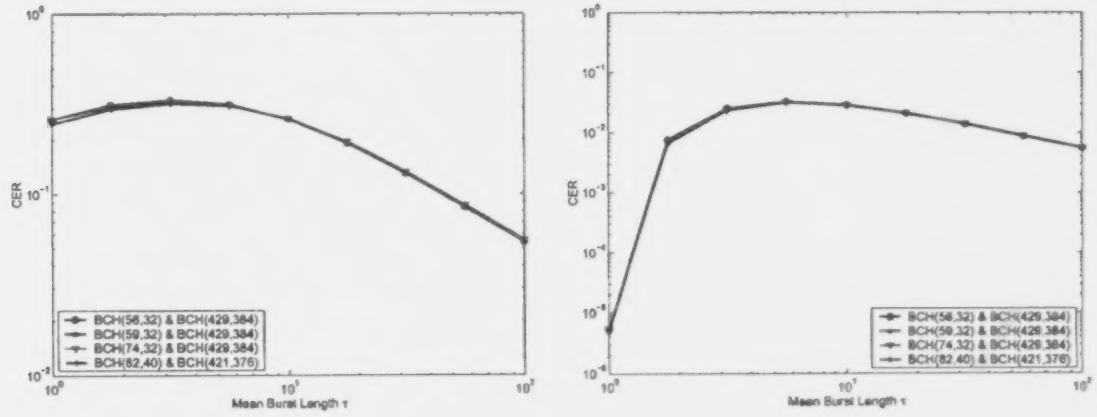
Note that the GTE scheme and the (74,32) BCH header/(429,384) BCH payload code scheme have identical BW efficiencies. While the performance of the two schemes is almost identical, the GTE scheme with the shortest payload has the best CER and PBER performance and the (74,32) BCH header/(429,384) BCH payload code scheme with the shortest header has

the best CLR and PER performance.



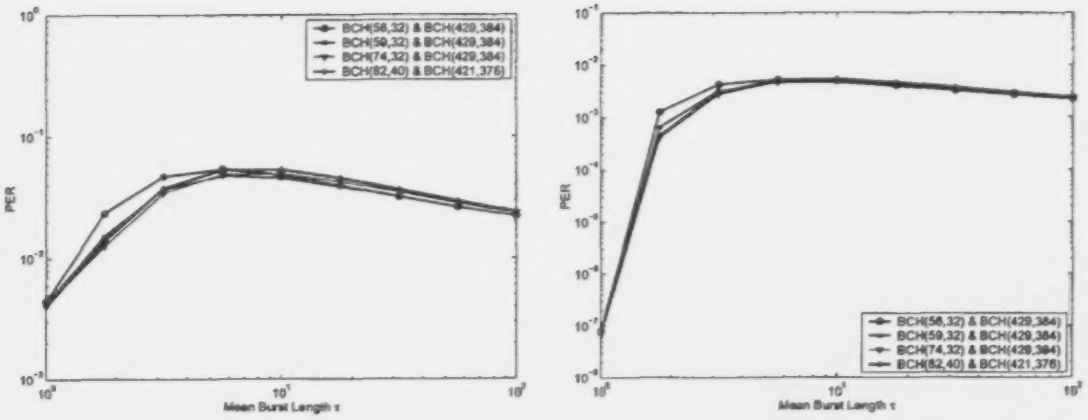
(a) CLR - BER = 10^{-2} *(b) CLR - BER = 10^{-3}*

Figure 47: Performance comparison of CLR for combination header/payload BCH codes.



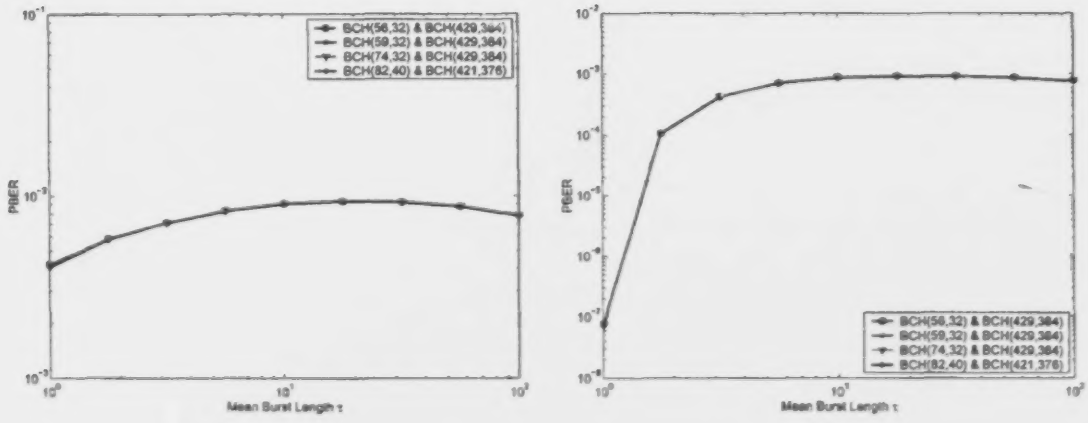
(a) CER - BER = 10^{-2} *(b) CER - BER = 10^{-3}*

Figure 48: Performance comparison of CER for combination header/payload BCH codes.



(a) PER - BER = 10^{-2} *(b) PER - BER = 10^{-3}*

Figure 49: Performance comparison of PER for combination header/payload BCH codes.



(a) PBER - BER = 10^{-2} *(b) PBER - BER = 10^{-3}*

Figure 50: Performance comparison of PBER for combination header/payload BCH codes.

5.5 Duplicate-Header Scheme

The DERA proposal uses duplicate headers for protection against errors with the second header being appended at the end of the standard ATM cell. In the most simple case, the second header is an exact duplicate of the standard ATM cell header. The resulting wireless ATM cell structure is shown in Fig. 51, where field F_0 represents the first header ($N_0 = 40$, t_0), F_1 represents the cell payload ($N_1 = 384$, $t_1 = 0$) and F_2 represents the second header ($N_2 = N_0$, $t_2 = t_0$). The error-correcting capability of the CRC header code used in standard ATM is $t_0 = t_2 = 1$ if HEC is used in correction mode, or $t_0 = t_2 = 0$ if HEC applies error detection only. Assuming that a cell with duplicate headers is dropped (lost) when the number

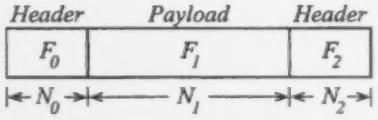


Figure 51: Wireless ATM cell structure for the DERA error-control proposal.

of errors exceeds the code error-correcting capability for both headers, i.e., when $\{U_0 > t_0\}$ and $\{U_2 > t_2\}$, the performance metrics of interest are given by:

$$\text{CLR} = \Pr\{U_0 > t_0, U_2 > t_2\} = \sum_{k_0=t_0+1}^{N_0} \sum_{k_1=0}^{N_1} \sum_{k_2=t_2+1}^{N_2} \psi(k_0, k_1, k_2) \tag{49a}$$

$$\begin{aligned} \text{CER} &= \text{CLR} + \Pr\{U_0 \le t_0, U_1 > t_1\} + \Pr\{U_0 > t_0, U_1 > t_1, U_2 \le t_2\} \\ &= \text{CLR} + \sum_{k_0=0}^{t_0} \sum_{k_1=t_1+1}^{N_1} \sum_{k_2=0}^{N_2} \psi(k_0, k_1, k_2) + \sum_{k_0=t_0+1}^{N_0} \sum_{k_1=t_1+1}^{N_1} \sum_{k_2=0}^{t_2} \psi(k_0, k_1, k_2) \end{aligned} \tag{49b}$$

$$\text{PER} = \text{CLR} + \text{PER}_2 \tag{49c}$$

$$\begin{aligned} \text{PBER} &= \frac{\text{PER}_2}{\Pr\{U_0 \le t_0\} + \Pr\{U_0 > t_0, U_2 \le t_2\}} \\ &= \frac{\text{PER}_2}{\sum_{k_0=0}^{t_0} \sum_{k_1=0}^{N_1} \sum_{k_2=0}^{N_2} \psi(k_0, k_1, k_2) + \sum_{k_0=t_0+1}^{N_0} \sum_{k_1=0}^{N_1} \sum_{k_2=0}^{t_2} \psi(k_0, k_1, k_2)}, \end{aligned} \tag{49d}$$

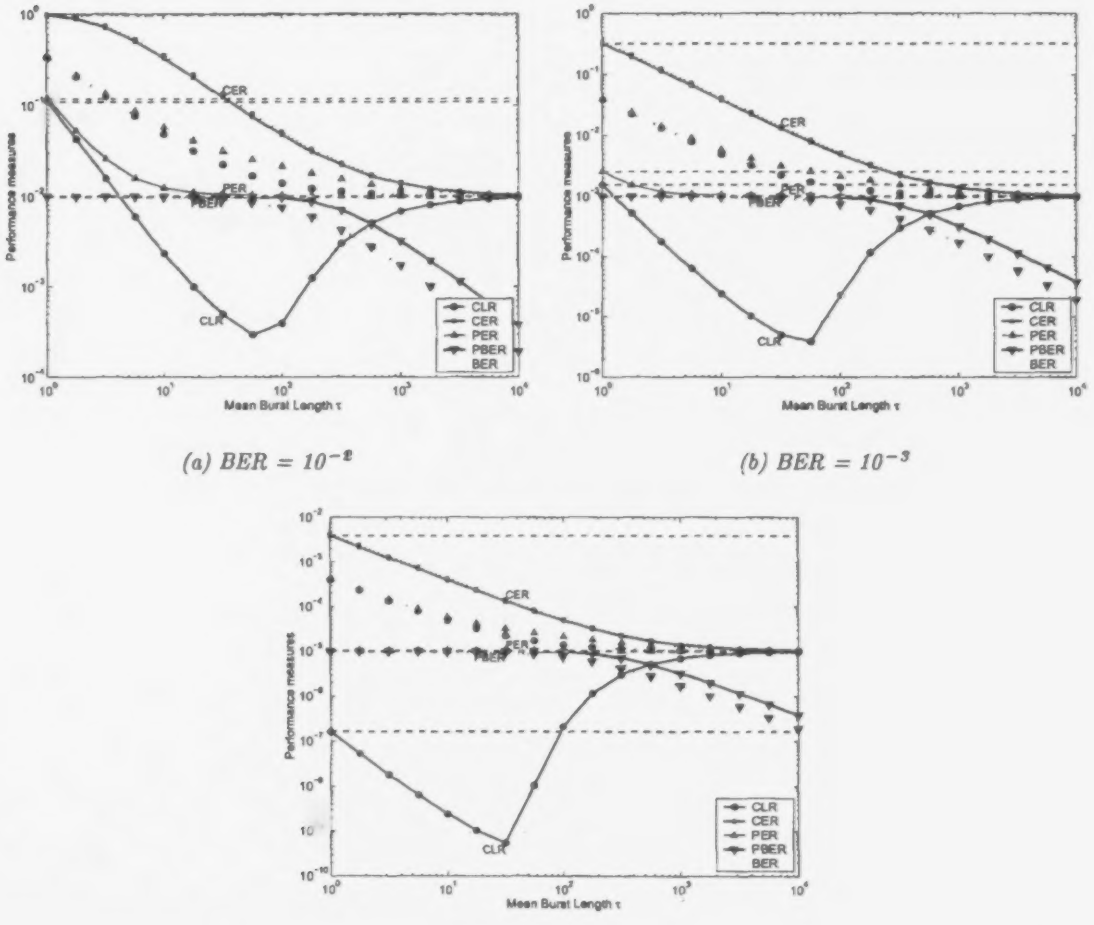
where PER_2 is the payload-error rate of the undiscarded ATM cells and is given by

$$\begin{aligned} \text{PER}_2 &= \sum_{k_1=t_1+1}^{N_1} \frac{k_1}{N_1} \Big[\Pr\{U_0 \le t_0, U_1 = k_1\} + \Pr\{U_0 > t_0, U_1 = k_1, U_2 \le t_2\} \Big] \\ &= \sum_{k_0=0}^{t_0} \sum_{k_1=t_1+1}^{N_1} \sum_{k_2=0}^{N_2} \frac{k_1}{N_1} \psi(k_0, k_1, k_2) + \sum_{k_0=t_0+1}^{N_0} \sum_{k_1=t_1+1}^{N_1} \sum_{k_2=0}^{t_2} \frac{k_1}{N_1} \psi(k_0, k_1, k_2). \end{aligned} \tag{49e}$$

5.5.1 Performance of DERA Scheme in Error-Detection Mode

Analytical results for the duplicate-header scheme when the HEC operates in detection mode (no header-error correction) are shown in Fig. 52 for different values of BER. The dotted lines in

the figure correspond to the performance measures for standard ATM with error detection. As can be seen from the figure, compared to standard ATM, the DERA scheme provides improved performance with respect to CLR and PER, no significant improvement with respect to CER and a slight degradation with respect to PBER.



(a) BER = 10^{-2}

(b) BER = 10^{-3}

(c) BER = 10^{-5}

Figure 52: Analytical results for the DERA duplicate-header scheme over the GE channel in HEC detection mode (payload size = 384).

Note that the performance behavior of the CLR as a function of the mean burst length τ for this scheme is distinctly different from that for standard ATM and the other FEC schemes considered so far. In the previous schemes, for values of τ large enough, CLR takes values higher than the BER to which it converges in the limit as $\tau \to \infty$. In the DERA scheme, the CLR also converges to the BER as τ increases but in this case, the limit is approached from values that are lower than the BER.

An expression for the CLR in the case of standard ATM cell headers with error detection

can be easily obtained from Eq. 49a. Let H_1 denote the event that the first header of the wireless ATM cell (field F_1) is not corrupted by errors:

$$H_1 \equiv \{F_1 \text{ free of errors}\}.$$

Then, $H_1^c = \{F_1 \text{ in error}\}$ and $\Pr(H_1^c) = 1 - \Pr(H_1)$. Similarly, for the second header,

$$H_2 \equiv \{F_2 \text{ free of errors}\}, \qquad H_2^c = \{F_2 \text{ in error}\}$$

and $\Pr(H_2^c) = 1 - \Pr(H_2)$. CLR is given by

$$\text{CLR} = \Pr(H_1^c H_2^c) = 1 - \Pr(H_1^c H_2) - \Pr(H_1 H_2^c) - \Pr(H_1 H_2), \tag{50}$$

where

$$\begin{aligned}
\Pr(H_1^c H_2) &= \boldsymbol{\pi} \sum_{k_0=1}^{N_0} \boldsymbol{\Phi}(k_0, N_0) \sum_{k_1=0}^{N_1} \boldsymbol{\Phi}(k_1, N_1) \boldsymbol{\Phi}(0, N_0)\mathbf{e} \\
&= \boldsymbol{\pi}[\mathbf{P}^{N_0} - \boldsymbol{\Phi}(0, N_0)]\mathbf{P}^{N_1}\boldsymbol{\Phi}(0, N_0)\mathbf{e} \\
&= \boldsymbol{\pi}[\mathbf{I} - \boldsymbol{\Phi}(0, N_0)]\mathbf{P}^{N_1}\boldsymbol{\Phi}(0, N_0)\mathbf{e} \\
&= \boldsymbol{\pi}\boldsymbol{\Phi}(0, N_0)\mathbf{e} - \boldsymbol{\pi}\boldsymbol{\Phi}(0, N_0)\mathbf{P}^{N_1}\boldsymbol{\Phi}(0, N_0)\mathbf{e} \\
&= \Pr(H_1 H_2^c)
\end{aligned} \tag{51}$$

and

$$\Pr(H_1 H_2) = \boldsymbol{\pi}\boldsymbol{\Phi}(0, N_0)P^{N_1}\boldsymbol{\Phi}(0, N_0)\mathbf{e}. \tag{52}$$

For the GE channel with transition probability matrix $\mathbf{P}$ and error-rate matrix $\mathbf{P_e}$ given by

$$\mathbf{P} = \begin{bmatrix} 1-\alpha/\tau & \alpha/\tau \\ 1/\tau & 1-1/\tau \end{bmatrix} \text{ and } \mathbf{P_e} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix},$$

the quantities $\Pr(H_1) = \Pr(H_2)$ and $\Pr(H_1 H_2)$ are expressed in terms of p, τ, N_0 and N_1 as follows:

$$\Pr(H_1) = \boldsymbol{\pi}\boldsymbol{\Phi}(0, N_0)\mathbf{e} = \frac{(1-\alpha/\tau)^{N_0-1}}{1+\alpha} \tag{53}$$

$$\Pr(H_1 H_2) = \boldsymbol{\pi}\boldsymbol{\Phi}(0, N_0)P^{N_1}\boldsymbol{\Phi}(0, N_0)\mathbf{e} = \left[\frac{(1-\alpha/\tau)^{N_0-1}}{1+\alpha}\right]^2 \left[1 + \alpha\left(1 - \frac{1+\alpha}{\tau}\right)^{N_1+1}\right], \tag{54}$$

where $\alpha = p/(1-p)$. An explicit expression for CLR in terms of p, τ, N_0 and N_1 can be obtained by substituting for $\boldsymbol{\pi}\boldsymbol{\Phi}(0, N_0)\mathbf{e}$ and $\boldsymbol{\pi}\boldsymbol{\Phi}(0, N_0)P^{N_1}\boldsymbol{\Phi}(0, N_0)\mathbf{e}$ from Eqs. 53 and 54 in Eqs. 51, 52 and 50:

$$\begin{aligned}
\text{CLR} &= 1 - 2\boldsymbol{\pi}\boldsymbol{\Phi}(0, N_0)\mathbf{e} + \boldsymbol{\pi}\boldsymbol{\Phi}(0, N_0)P^{N_1}\boldsymbol{\Phi}(0, N_0)\mathbf{e} \\
&= 1 - 2\frac{(1-\alpha/\tau)^{N_0-1}}{1+\alpha} + \left[\frac{(1-\alpha/\tau)^{N_0-1}}{1+\alpha}\right]^2 \left[1 + \alpha\left(1 - \frac{1+\alpha}{\tau}\right)^{N_1+1}\right] \qquad (55) \\
&= \alpha\left[\frac{(1-\alpha/\tau)^{N_0-1}}{1+\alpha}\right]^2 \left[1 - \frac{1+\alpha}{\tau}\right]^{N_1+1} + \left[1 - \frac{(1-\alpha/\tau)^{N_0-1}}{1+\alpha}\right]^2. \qquad (56)
\end{aligned}$$

Initially, CLR decreases with τ, it achieves a minimum value CLR_{min} for some value $\tau = \tau_{clr}$ and increases with τ for large values of τ. This can be explained as follows. A cell is lost whenever both headers are corrupted by errors. For error-bursts that are short compared to the cell size ($\tau << N_1$), the two headers in a cell can be corrupted simultaneously by separate bursts only. For a fixed BER, as the burst length increases, the gap between bursts also increases and, therefore, the probability of both headers in a cell being corrupted by errors, i.e., the CLR, decreases. This trend of the CLR performance, that is, the decrease with burst length, is present for burst lengths up to the threshold value τ_{clr}. Any further increase of the burst length to values high enough to have both headers in a cell corrupted by a single burst ($\tau >> N_1$), will result in the increase of the CLR. In this case, the longer the error-burst, the higher the probability of both headers in a cell being corrupted by errors and the higher the CLR. Summarizing, CLR decreases with τ for small values of the ratio τ/N_1 and increases with τ for large values of τ/N_1.

In mathematical terms, the CLR performance is dominated by the second term in Eq. 56 for $\tau < \tau_{clr}$,

$$\mathrm{CLR} = \Pr(H_1^c H_2^c) \approx \left[1 - \frac{(1-\alpha/\tau)^{N_0-1}}{1+\alpha}\right]^2 = \Pr(H_1^c)\Pr(H_2^c), \tag{57}$$

and dominated by the first term in Eq. 56 for $\tau > \tau_{clr}$,

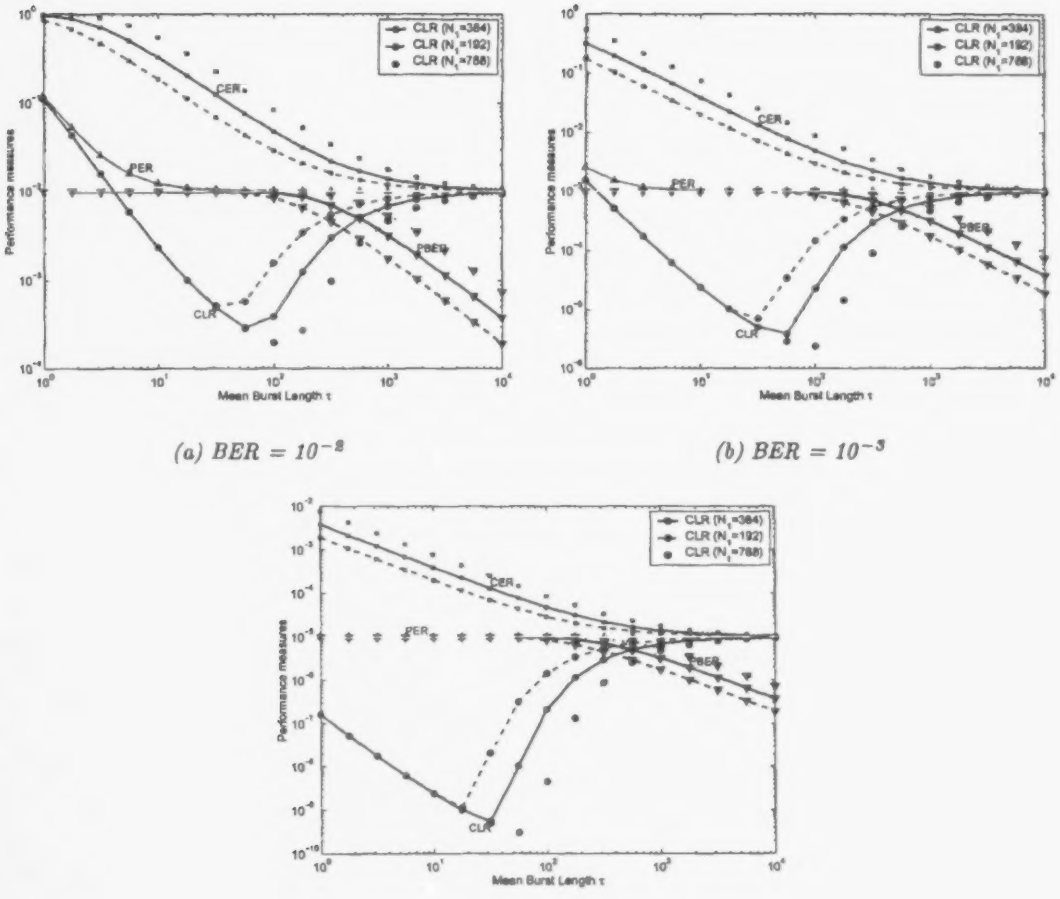
$$\mathrm{CLR} = \Pr(H_1^c H_2^c) \approx \alpha \left[\frac{(1-\alpha/\tau)^{N_0-1}}{1+\alpha}\right]^2 \left[1 - \frac{1+\alpha}{\tau}\right]^{N_1+1}. \tag{58}$$

The CER, PER and PBER are monotone decreasing functions of τ.

Performance depends on the size of the payload N_1 as shown in the results presented in Fig. 53 for different values of N_1, $N_1 = 192, 384, 768$. The solid curves in Fig. 53 are for the results obtained for $N_1 = 384$, the dashed curves for the results obtained for $N_1 = 192$ and the dotted curves for the results obtained for $N_1 = 768$.

More specifically, for values of τ sufficiently small, the value of CLR does not vary with payload size N_1. In this range of τ, CLR is given by Eq. 57 and is clearly independent of N_1. For large values of τ, the value of CLR decreases with the increase of payload size N_1. For a given value of τ, the increase of payload size results in the increase of the separation between the two headers. This, in turn, results in the decrease of the probability that a single burst will corrupt both headers in a cell, i.e., it results in the decrease of the CLR. This is also evident from Eq. 58, since $0 < 1 - (1+\alpha)/\tau < 1$ in this range of τ. Clearly, τ_{clr} increases with N_1. In addition, CLR_{min} decreases with N_1. In other words, the use of larger payload size is preferable with respect to CLR performance. However, larger payload size results in higher CER and PBER over the entire range of τ. The PER remains unaffected by the payload size for the values of N_1 under consideration.

The CLR performance depends on the separation between the two headers. If the second header follows directly after the first header instead of being appended at the end of the payload (Fig. 54) the performance of the duplicate-header scheme may differ significantly as shown in Fig. 55 where the results obtained for the DERA proposal (dashed lines) are compared to those obtained for the scenario shown in Fig. 54 (solid lines). In this case, the CLR is identical to



(a) BER = 10^{-2}

(b) BER = 10^{-3}

(c) BER = 10^{-5}

Figure 53: Analytical results for the DERA duplicate-header scheme over the GE channel in HEC detection mode for different values of payload size N_1.

that obtained for the DERA proposal (Fig. 51) if the payload size is considered to be $N_1 = 0$:

$$\begin{aligned} \mathrm{CLR} &= 1 - 2\boldsymbol{\pi}\boldsymbol{\Phi}(0, N_0)\mathbf{e} + \boldsymbol{\pi}\boldsymbol{\Phi}(0, N_0)\boldsymbol{\Phi}(0, N_0)\mathbf{e} \\ &= 1 - 2\frac{(1-\alpha/\tau)^{N_0-1}}{1+\alpha} + \left[\frac{(1-\alpha/\tau)^{N_0-1}}{1+\alpha}\right]^2 (1+\alpha)\left(1-\frac{\alpha}{\tau}\right) \end{aligned} \tag{59}$$

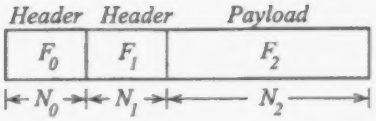
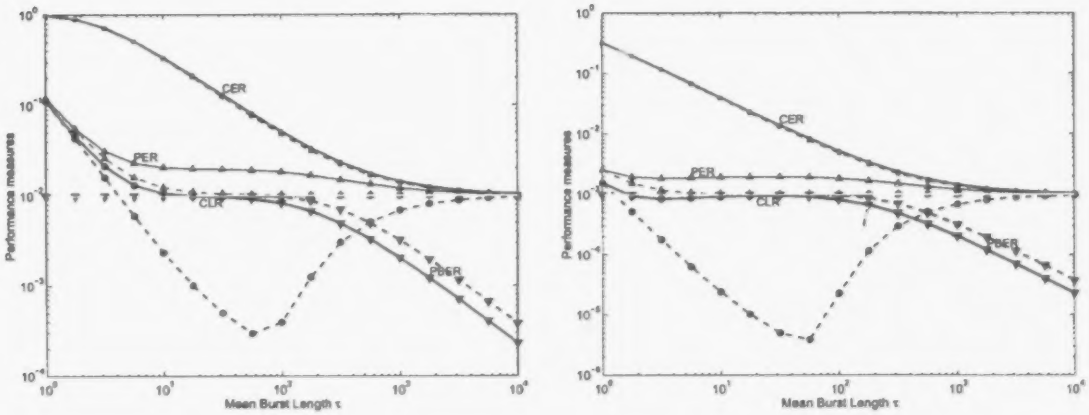
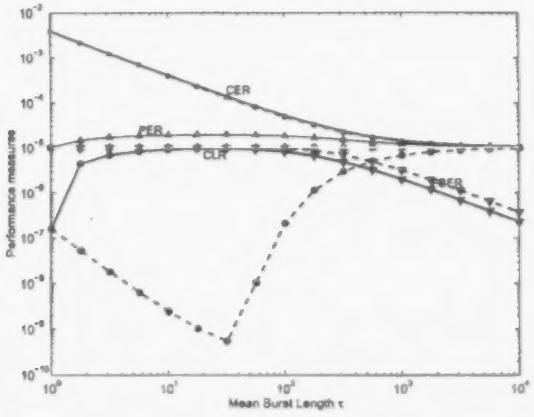


Figure 54: Wireless ATM cell structure for the duplicate-header control scheme (scenario 2).



(a) BER = 10^{-2}

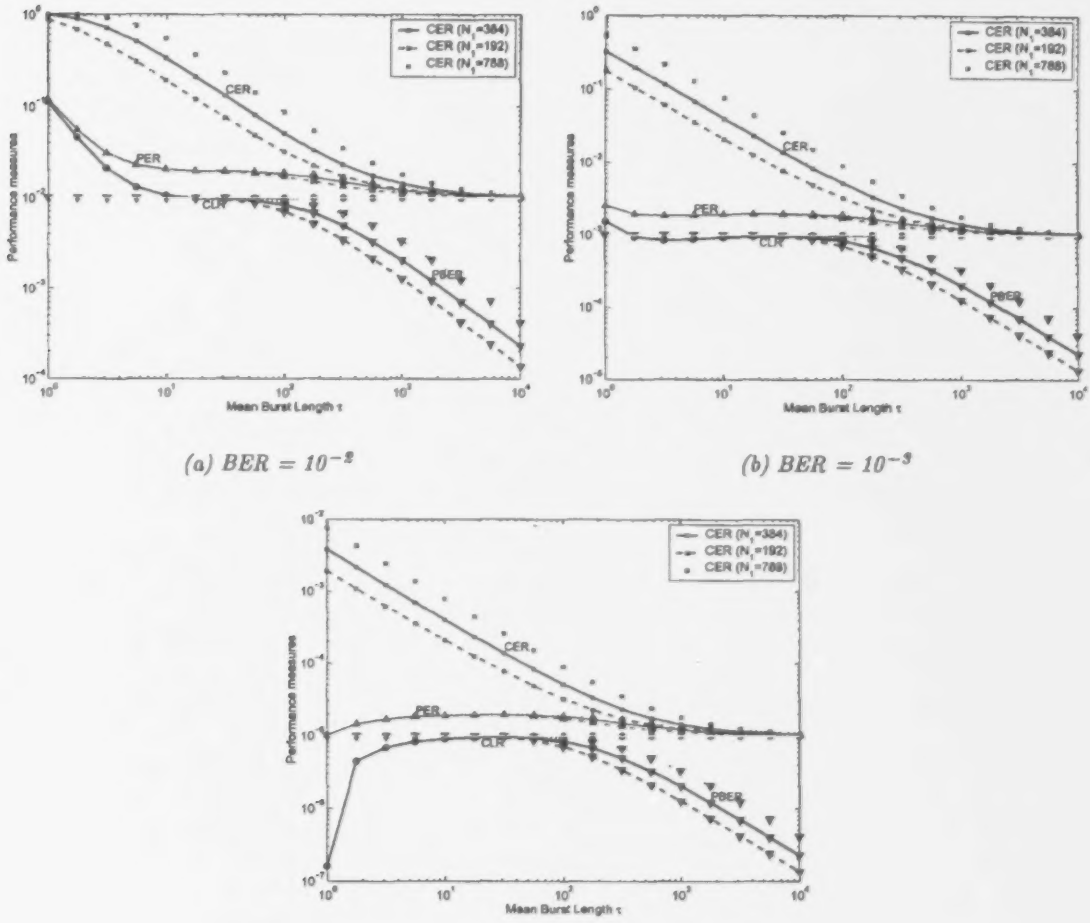
(b) BER = 10^{-3}



(c) BER = 10^{-5}

Figure 55: Analytical results for different scenarios of the duplicate-header scheme over the GE channel in HEC detection mode (payload size = 384).

The performance behavior of scenario 2 for the duplicate-header scheme with increasing payload size N_1 illustrated in Fig. 56 is similar to that observed for the DERA scheme (Fig. 53).



(a) BER = 10^{-2}

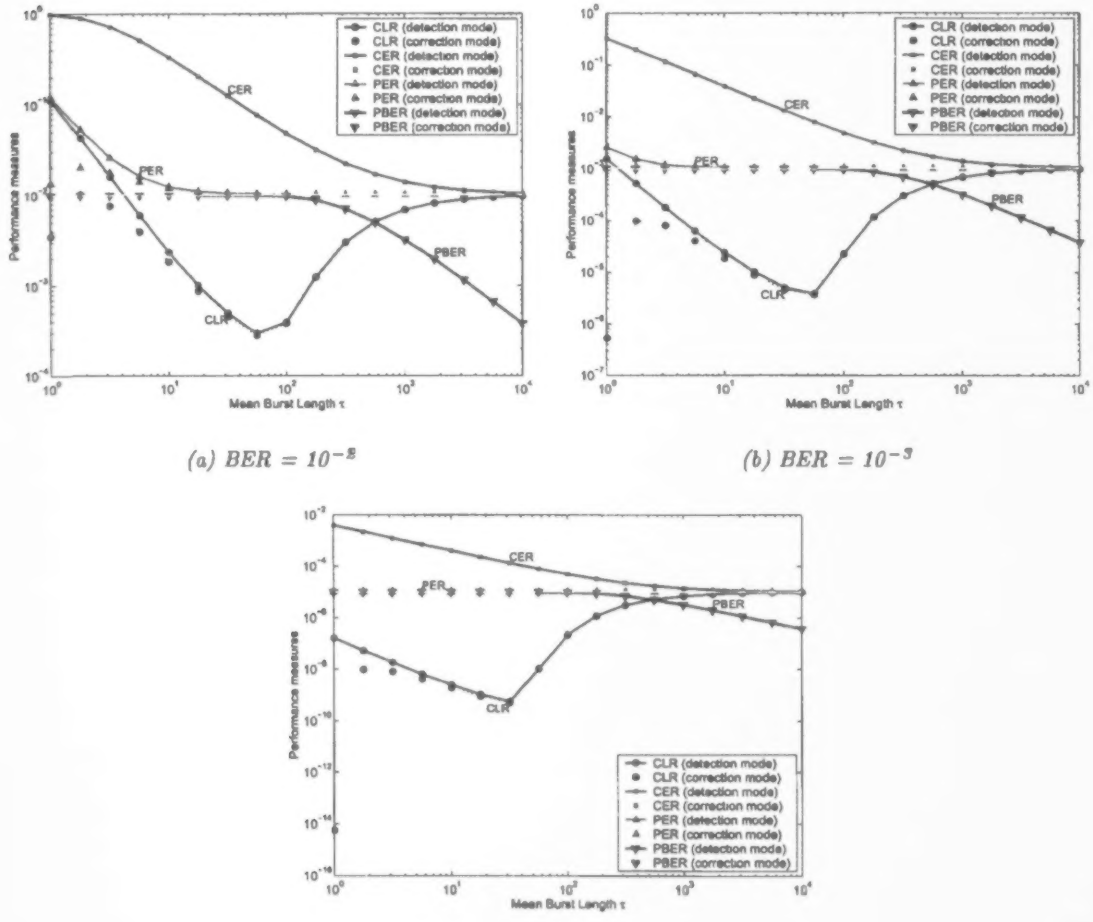
(b) BER = 10^{-3}

(c) BER = 10^{-5}

Figure 56: Analytical results for the duplicate-header scheme (scenario 2) over the GE channel in HEC detection mode for different values of payload size N_1.

5.5.2 Performance of DERA Scheme in Error-Correction Mode

The effect of using HEC in correction rather than detection mode on the performance of the DERA scheme is illustrated in Fig. 57. The use of the single-error-correcting capability of the standard ATM HEC results mainly in improved CLR performance for small values of τ. It also results in slightly improved PER performance for high BERs. The other performance metrics remain unaffected by the use of correction mode.



(a) BER = 10^{-2}

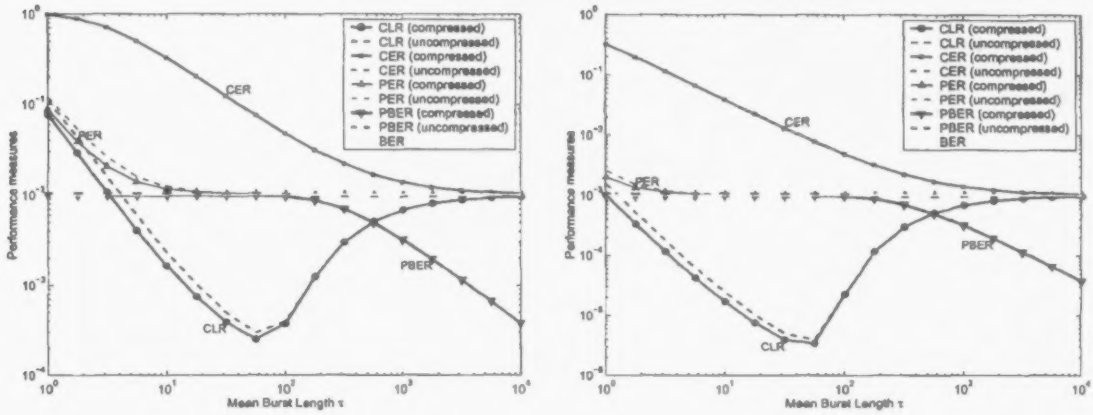
(b) BER = 10^{-3}

(c) BER = 10^{-5}

Figure 57: Analytical results for the DERA duplicate-header scheme over the GE channel in HEC correction mode (payload size = 384).

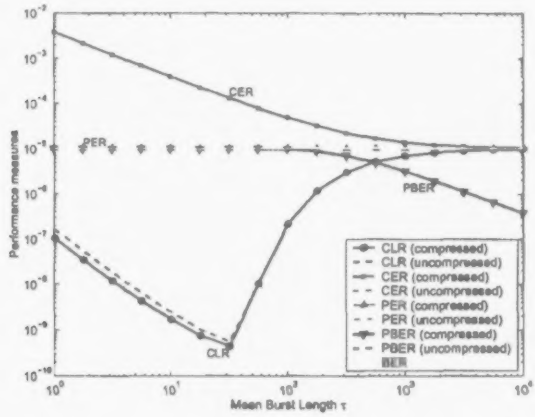
5.5.3 Performance of DERA Scheme with Compressed Headers

It can be easily proven that the CLR (Eq. 56) is an increasing function of the header size N_0. Therefore, improved CLR performance can be achieved by reducing the size of the cell headers. Specifically, the standard ATM cell header can be compressed by reducing the size of the VPI/VCI fields, which implies the reduction of the maximum number of ATM connections supported over radio links. Due to the bandwidth-limited nature of the wireless medium, the compression of the VPI/VCI fields has no significant practical implications; the number of ATM connections carried over radio links will be much smaller than the number of connections carried over fixed, high-bandwidth links.



(a) BER = 10^{-2}

(b) BER = 10^{-3}

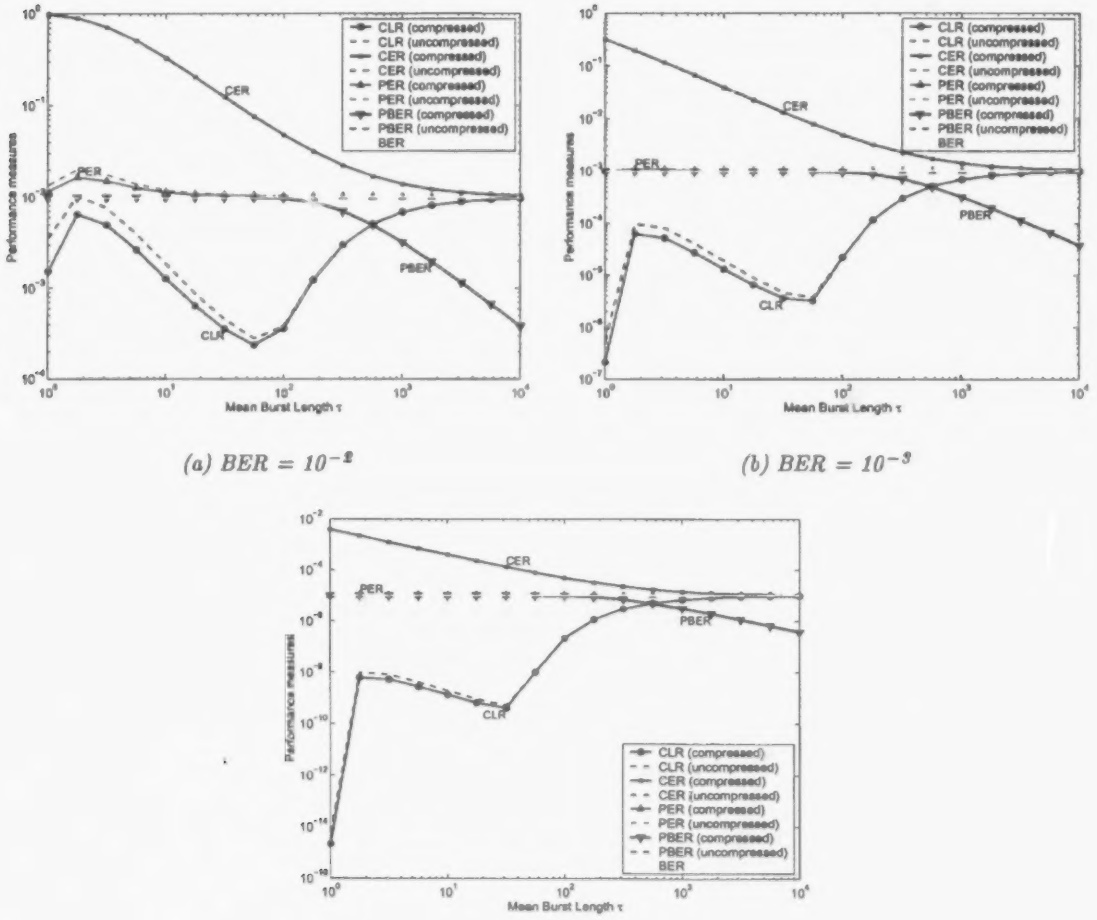


(c) BER = 10^{-5}

Figure 58: Analytical results for the DERA duplicate-header scheme over the GE channel in HEC detection mode (compressed headers).

Analytical results for such a scheme, where the VPI/VCI field size has been reduced by one byte compared to standard ATM, are shown in Figs. 58 and 59 for operation in HEC detection

and correction mode, respectively. The compressed header (24 bytes) is encoded using the standard ATM CRC-8 code.



(a) BER = 10^{-2}

(b) BER = 10^{-3}

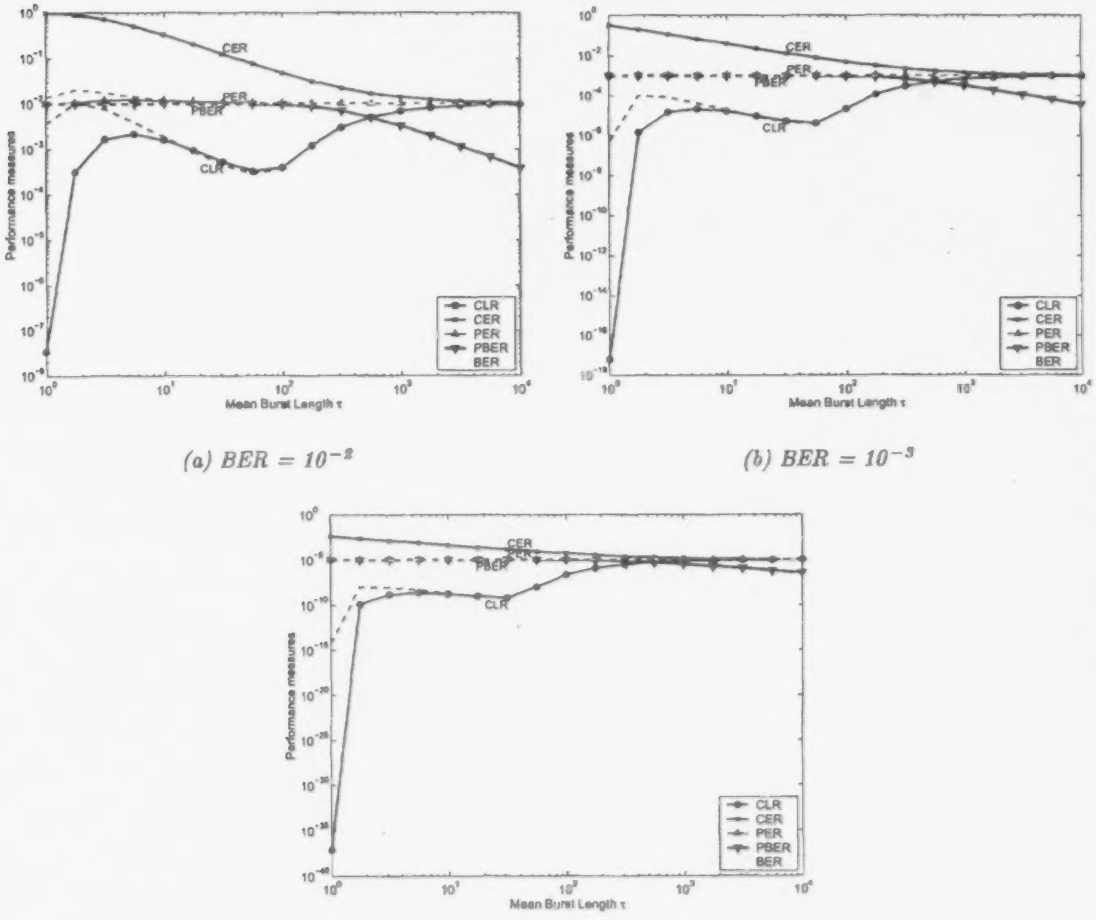
(c) BER = 10^{-5}

Figure 59: Analytical results for the DERA duplicate-header scheme over the GE channel in HEC correction mode (compressed headers).

A slight improvement in CLR and PER performance, due to header compression, can be observed in the lower range of values of τ for both HEC operation modes. The CER and PBER performance remains unaffected by header compression.

5.5.4 Performance of Duplicate-Header Scheme with BCH-Encoded Headers

A variant of the DERA scheme where ATM headers are encoded using BCH codes rather than the standard ATM CRC-8 code is considered in this section. The performance of a scheme that uses a (56,32) BCH header code is shown in Fig. 60. The results for the DERA variant with BCH-encoded headers are indicated by solid lines, whereas the results for the DERA scheme with error correction are indicated by dashed lines.



(a) BER = 10^{-2}

(b) BER = 10^{-3}

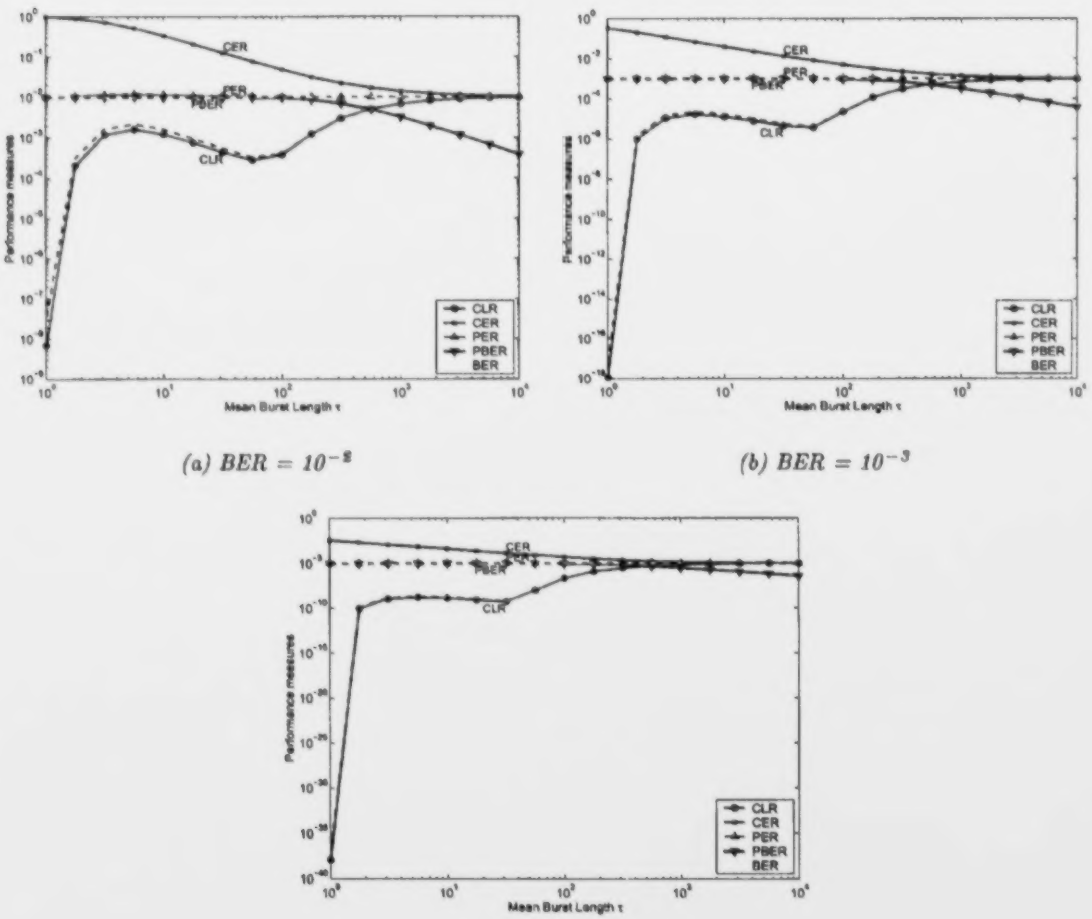
(c) BER = 10^{-5}

Figure 60: Analytical results for the duplicate-header scheme over the GE channel with (56,32) BCH header code.

The use of BCH header codes improves the CLR performance for small values of τ ($\tau < 10$) but has no significant impact on the rest of the performance measures.

5.5.5 Performance of Duplicate-Header Scheme with BCH-Encoded Compressed Headers

A slight improvement in the CLR performance is achieved if BCH encoding is applied to the compressed header. In Fig. 61, results are shown for the (48,24) BCH code of error-correcting capability $t = 4$ used in the case of a 24-bit compressed header (solid lines). Results are also shown for the case of the 32-bit uncompressed header and the (56,32) BCH code, also of error-correcting capability $t = 4$, considered in the previous subsection (dashed lines).



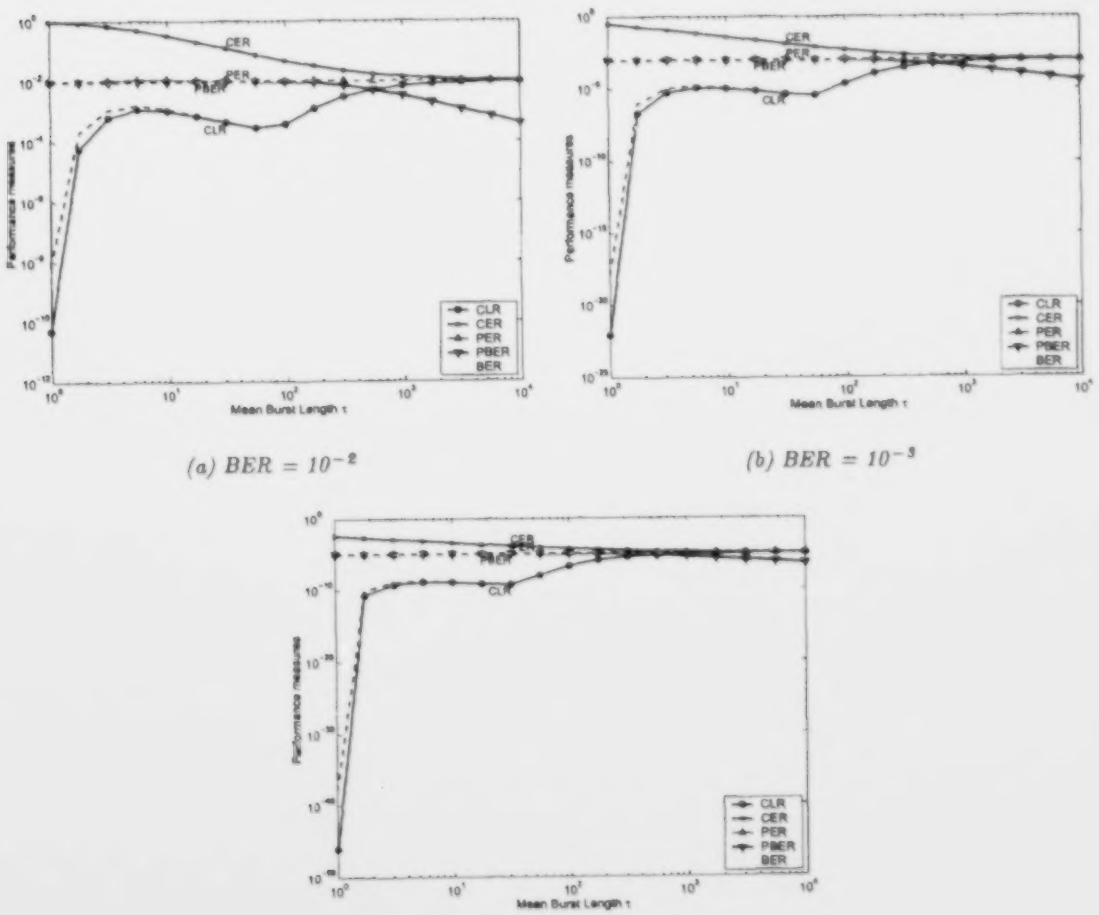
(a) BER = 10^{-2}

(b) BER = 10^{-3}

(c) BER = 10^{-5}

Figure 61: Analytical results for the duplicate-header scheme over the GE channel with (48,24) BCH header code.

An additional slight improvement in CLR and PER performance is achieved by increasing the error-correcting capability of the BCH code applied to the compressed header. For example, the results for the (51,24) BCH code with error-correcting capability $t = 5$ are shown in Fig. 62 (solid lines). The results for the (48,24) BCH code with error-correcting capability $t = 4$ are also shown in the same figure for comparison purposes (dashed lines).



(a) BER = 10^{-2}

(b) BER = 10^{-3}

(c) BER = 10^{-5}

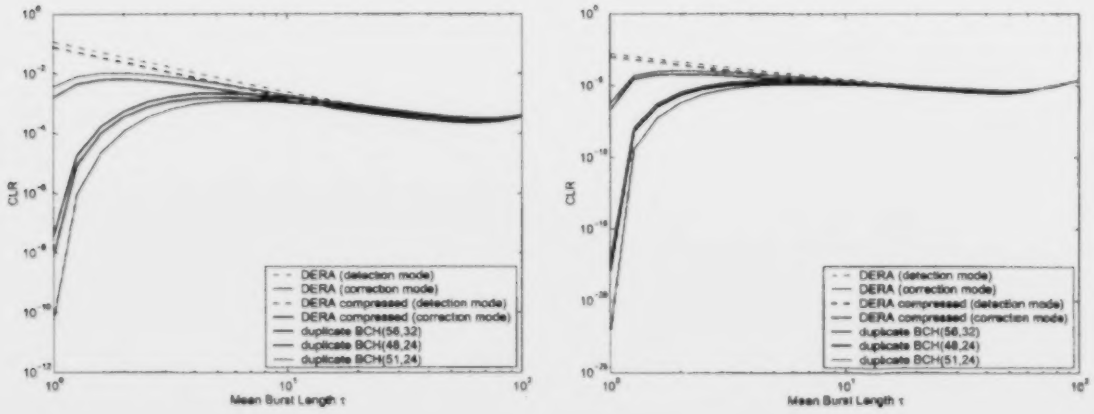
Figure 62: Analytical results for the duplicate-header scheme over the GE channel with (51,24) BCH header code.

5.5.6 Performance Comparison of Duplicate-Header Schemes

The performance behavior of the duplicate-header schemes with respect to the CLR, CER, PER and PBER performance measures is summarized in Figs. 63-66. Results are shown for BER values $p = 10^{-2}, 10^{-3}$. The results for $p = 10^{-5}$ follow a trend similar to that displayed by the results for $p = 10^{-3}$.

The following characteristics can be observed with respect to the different measures:
- **CLR** (Fig. 63)

- The schemes with BCH-encoded headers have improved CLR performance compared to the schemes with CRC encoded headers for small values of τ ($\tau < 10$).
- The schemes with compressed headers perform better than the schemes with full length headers, the improvement being most noticeable for small values of τ.
- The duplicate-header scheme with (51,24) BCH header code outperforms the other schemes with BCH-encoded headers over the entire range of τ. It is outperformed only by the schemes with CRC encoded compressed headers for $\tau > 10$, yet the difference in performance is very small.



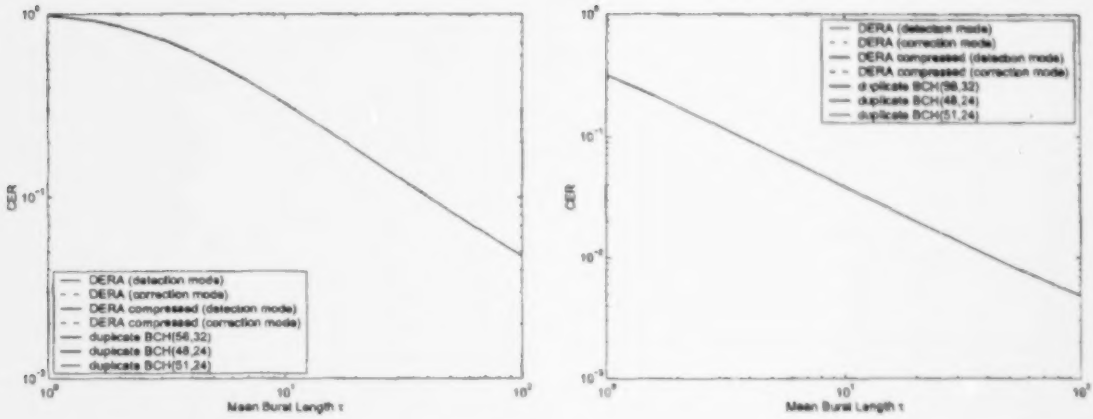
(a) BER = 10^{-2} *(b) BER = 10^{-3}*

Figure 63: Performance comparison of CLR for duplicate-header schemes.

- **CER** (Fig. 64)
All duplicate-header schemes under consideration have identical CER performance.

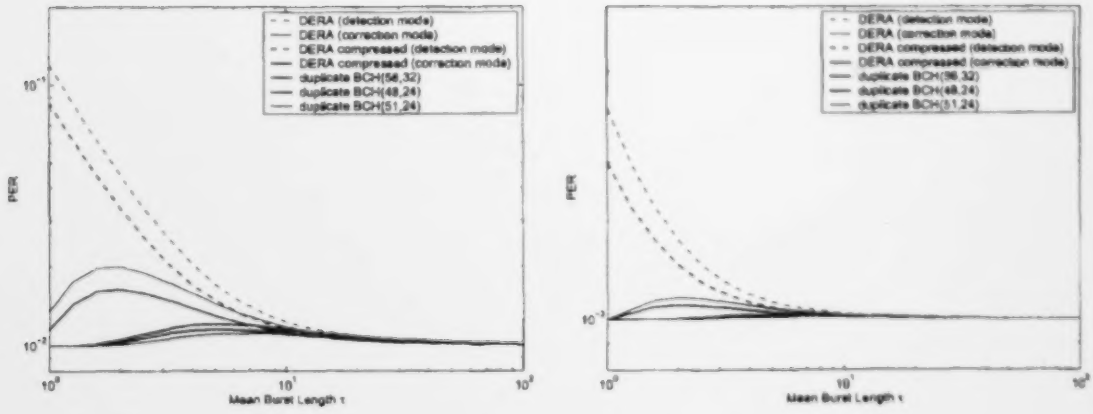
- **PER** (Fig. 65)
The PER performance of the schemes exhibits the same behavior described for the CLR.

- **PBER** (Fig. 66)
Similar to CER, all schemes yield almost identical PBER performance results.



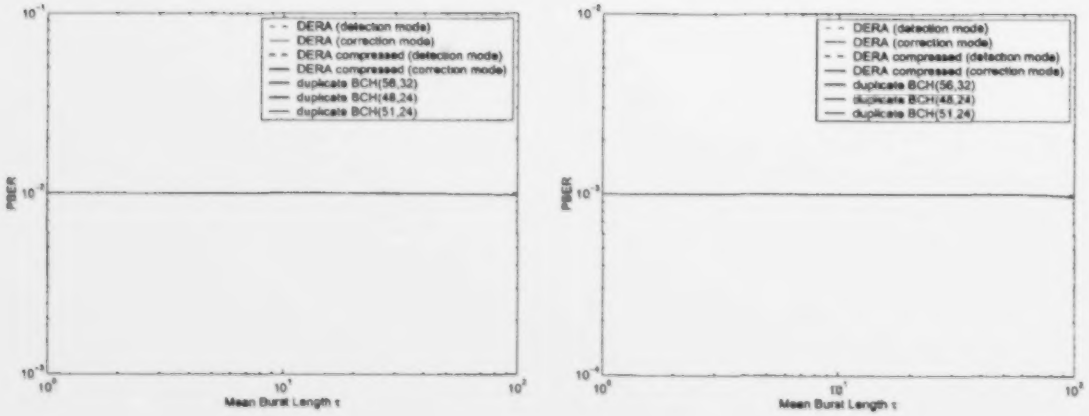
(a) BER = 10^{-2} *(b) BER = 10^{-3}*

Figure 64: Performance comparison of CER for duplicate-header schemes.



(a) BER = 10^{-2} *(b) BER = 10^{-3}*

Figure 65: Performance comparison of PER for duplicate-header schemes.



(a) $BER = 10^{-2}$ (b) $BER = 10^{-3}$

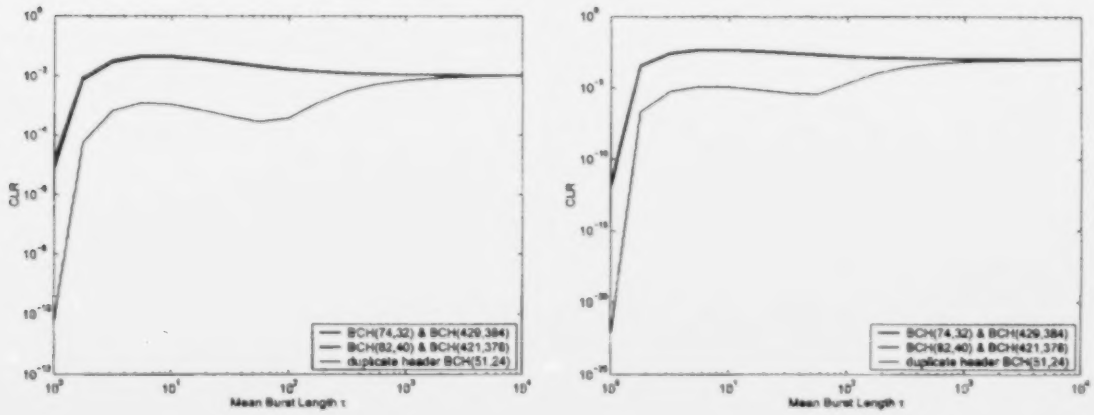
Figure 66: Performance comparison of PBER for duplicate-header schemes.

6 Recommendations for Error Control Over the Markov Error Channel

The performance results for the combination header/payload FEC schemes (Section 5.4.5) and the duplicate-header schemes (Section 5.5.6) are compared in this section. The (82,40) BCH header/(421,376) BCH payload code (GTE scheme) and the (74,32) BCH header/(429,384) BCH payload code were the two schemes that exhibited the best performance in the former category. The two schemes are of equal bandwidth efficiency $\eta = 0.763$ and have comparable performance. The duplicate-header scheme with compressed headers encoded using a (51,24) BCH header code had the best performance in the latter category. The BW efficiency of this scheme is $\eta = 384/(2 \times 51 + 384) = 0.79$.

Based on the results obtained for the three schemes, shown in Figs. 67-70, the following observations can be made regarding their relative performance:

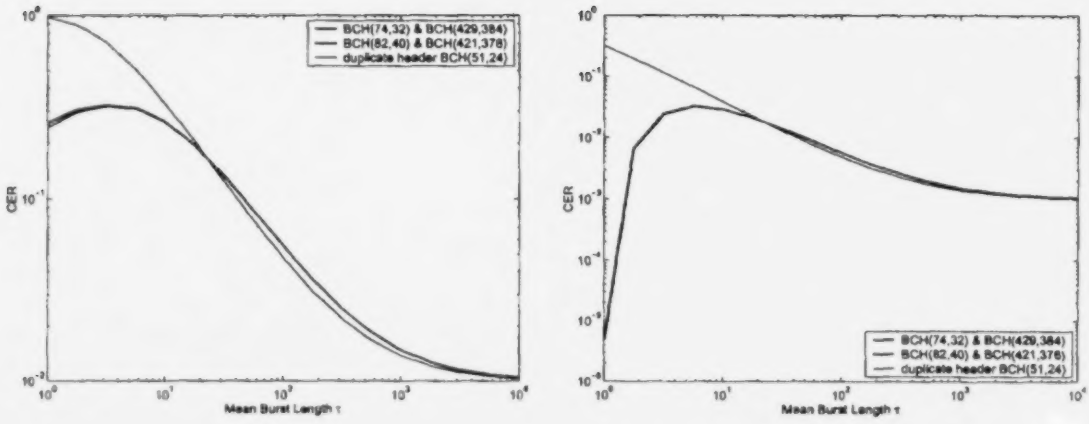
- The duplicate-header scheme outperforms the header/payload FEC schemes with respect to CLR. This difference can be as large as several orders of magnitude for $\tau < 100$.



(a) BER = 10^{-2} *(b) BER = 10^{-3}*

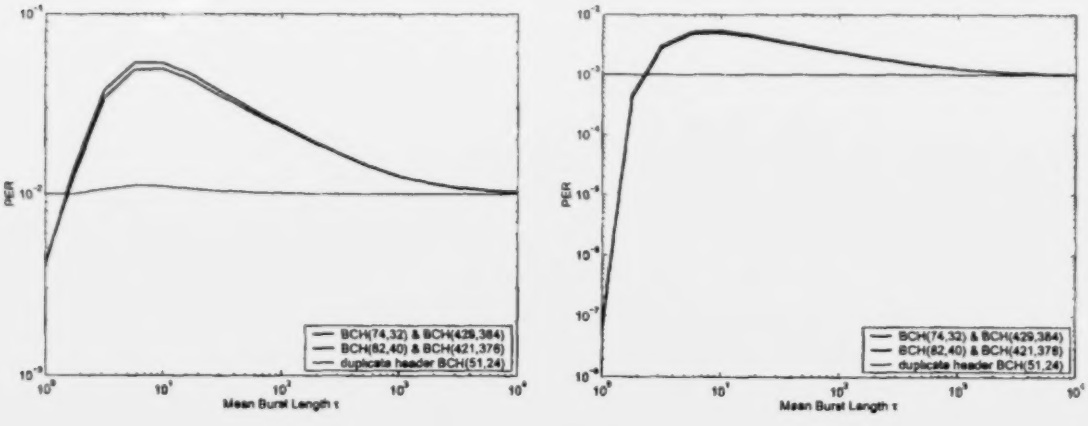
Figure 67: CLR performance comparison.

- The duplicate-header scheme is outperformed by the other schemes with respect to CER. The CER of the duplicate-header scheme is almost the same as that of standard ATM where no payload error control is applied. This is anticipated in view of the fact that no payload error control is used in the case of the duplicate-header scheme and because the CER is more sensitive to the encoding of the payload rather than of the header.
- The PER of the duplicate-header scheme is almost constant over the entire range of τ and equal to the BER p. The duplicate-header scheme outperforms the other schemes over the entire range of τ with the exception of very small values close to one.
- The PBER performance of the duplicate-header scheme is worse than that of the other schemes. In fact, it is worse than the performance of standard ATM. For small values of τ,



(a) BER = 10^{-2} *(b) BER = 10^{-3}*

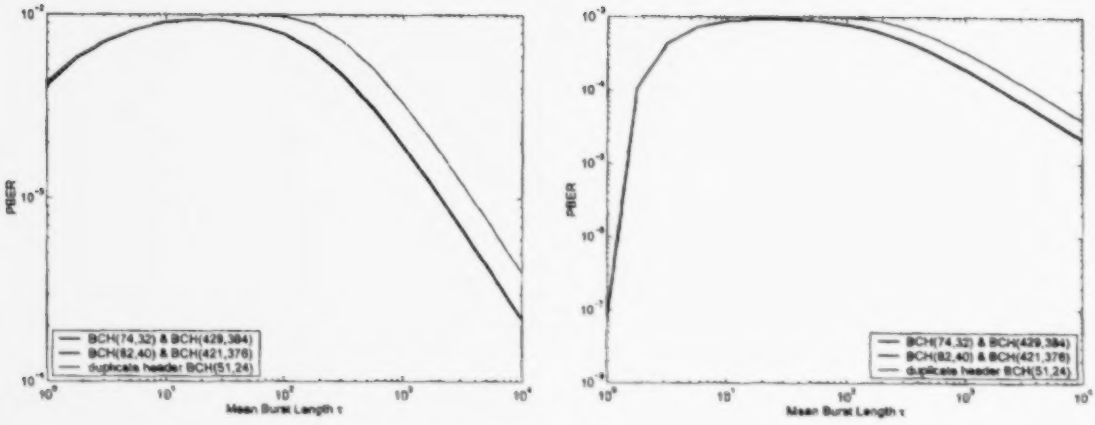
Figure 68: CER performance comparison.



(a) BER = 10^{-2} *(b) BER = 10^{-3}*

Figure 69: PER performance comparison.

the PBER performance of the combination schemes has a trend that is distinctly different from that of the duplicate-header scheme or of standard ATM. This is attributed to the effect of payload-error correction which prevails for small values of τ and p.



(a) BER = 10^{-2} *(b) BER = 10^{-3}*

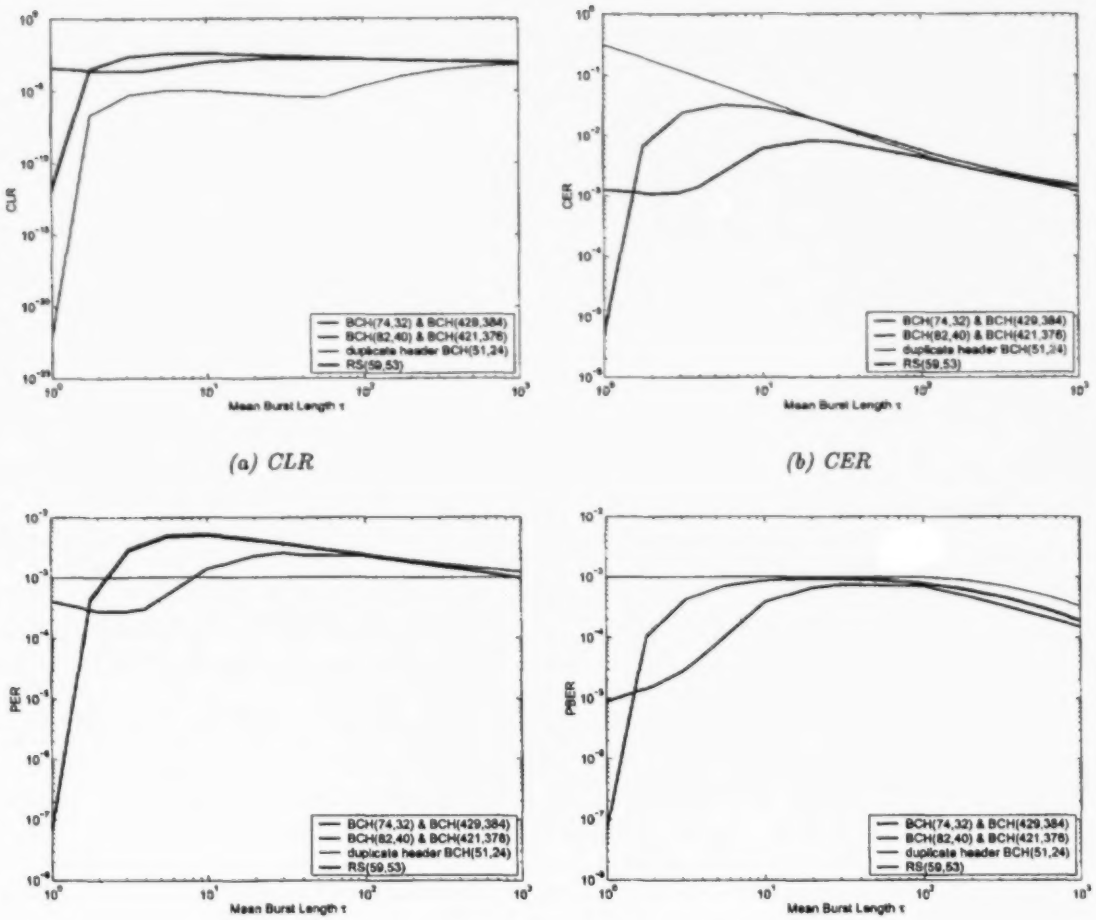
Figure 70: PBER performance comparison.

Finally, the performance results for the three schemes considered above are compared to the results for the (59,53) RS code in Fig. 71 for BER $p = 10^{-3}$. It is observed that:

- The duplicate-header scheme outperforms all other schemes with respect to CLR.
- The RS code exhibits the best CER performance over the entire range of τ except for $\tau = 1$ where it is outperfored by the combination header/payload FEC schemes. Similarly for the PBER performance.
- With respect to PER, the header/payload FEC schemes exhibit the best performance for $\tau = 1$, the RS code exhibits the best performance in the range between $\tau = 2$ and $\tau = 8$ and the duplicate-header scheme exhibits the best performance for $\tau > 8$.

The duplicate-header scheme with the best CLR performance is a good candidate for voice transport over the GE channel. Recall that this scheme does not apply payload-error control, and therefore, has a poor CER and PBER performance compared to the other schemes. However, given the voice tolerance to errors, it is preferable to have cells delivered with errors than to have a large number of lost cells. In addition, a payload-error control scheme could be used in combination with the duplicate-header scheme to improve the CER, PER and PBER performance at the expense of decreasing the code rate.

The RS code has some inherent desirable performance characteristics with respect to CER, PER and PBER for values of τ less than the code symbol length, but does not perform as well as the header/payload FEC schemes over the random-error channel ($\tau = 1$).



(a) CLR *(b) CER*

(c) PER *(d) PBER*

Figure 71: Performance comparison.

A Derivation of probabilities P_{dis} and P_{und}

Detection Mode

In detection mode, the probability of an undetected error event in a header, P_{und}, and the probability of a detected error event in a header (or cell discard probability), P_{dis}, can be expressed in terms of the codeword weight distribution, A_i, $i = 0, 1, \ldots, n$ [3] as follows:

$$\begin{aligned} P_{und} &= \Pr\{\text{undetected error in detection mode}\} \\ &= \sum_{i=1}^{n} A_i p^i (1-p)^{n-i}, \end{aligned} \tag{60}$$

$$\begin{aligned} P_{dis} &= \Pr\{\text{detected error in detection mode}\} \\ &= 1 - \Pr\{\text{no errors detected in detection mode}\} \\ &= 1 - \Pr\{\text{no errors incurred in detection mode}\} \\ &\quad - \Pr\{\text{undetected errors in detection mode}\} \\ &= 1 - (1-p)^n - \sum_{i=1}^{n} A_i p^i (1-p)^{n-i} \\ &= 1 - \sum_{i=0}^{n} A_i p^i (1-p)^{n-i}. \end{aligned} \tag{61}$$

Correction Mode

When the single-bit error-correcting capability of the HEC CRC code is applied, i.e., in correction mode, the probability of an undetected error event in a header, P'_{und}, and the probability of a detected error event in a header (or cell discard probability), P'_{dis}, are given by:

$$\begin{aligned} P'_{und} &= \Pr\{\text{undetected error in correction mode}\} \\ &= \Pr\{\text{undetected error in detection mode}\} \\ &\quad + \Pr\{\text{incorrect correction in correction mode}\} \\ &= P_{und} + \sum_{i=2}^{n} (i+1)\left[A_{i+1} + (n-i+1)A_{i-1}\right] p^i (1-p)^{n-i}, \end{aligned} \tag{62}$$

$$\begin{aligned} P'_{dis} &= \Pr\{\text{detected error in correction mode}\} \\ &= 1 - \Pr\{\text{no errors detected in correction mode}\} \\ &= 1 - \Pr\{\text{no errors detected in detection mode}\} \\ &\quad - \Pr\{\text{corrected errors in correction mode}\} \\ &= P_{dis} - np(1-p)^{n-1}. \end{aligned} \tag{63}$$

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